2025 IEEE APCCAS

21st IEEE Asia Pacific Conference on Circuits and Systems

DATE

Oct 12-15, 2025

VENUE

Paradise Hotel Busan

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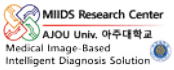

PROGRAM BOOK

2025 IEEE APCCAS

21st IEEE Asia Pacific Conference on Circuits and Systems

"Next-Generation Circuits and Systems from Silicon to Intelligence"

October 12-15, 2025

Paradise Hotel Busan, Busan, Korea

2025 IEEE
APCCAS
21st IEEE Asia Pacific Conference on Circuits and Systems

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FOREWORD "Welcome to APCCAS 2025"

General Chair
Kyung-Ki Kim,
Daegu University,
Korea

General Co-Chairs
Hyuk-Jae Lee,
Seoul National University,
Korea

Distinguished speakers, participants, and esteemed partners, we are delighted to welcome you to the IEEE Asia-Pacific Conference on Circuits and Systems (APCCAS 2025), held at the beautiful Paradise Hotel Busan in Busan, South Korea, October 12–15, 2025.

APCCAS serves as the premier regional forum where experts convene to exchange knowledge and drive progress in our field. This year's theme, "Next-Generation Circuits and Systems: From Silicon to Intelligence," addresses the pivotal technological shift we now face. The conference is strategically focused on defining the essential role that circuits and systems must play in the revolution led by artificial intelligence (AI) and future computing paradigms.

To that end, we have curated a comprehensive and diverse program designed to deliver both intellectual growth and tangible benefit. The program features visionary keynote presentations that provide high-level insights into the future roadmap for post-silicon technologies. In addition, we are pleased to host specialized events: the AutoCAS 2025 Workshop will explore critical circuits and systems for autonomous mobility—covering advanced sensing and V2X communications; the PrimeAsia Session offers a vital platform for recent postgraduate researchers to present their directions; dedicated Industrial Sessions showcase commercial innovation; and the Young Professionals (YP) program is designed to foster the next generation of leaders.

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Yoshifumi Nishio

Tokushima University,
Japan

General Co-Chairs
Kea-Tiong (Samuel) Tang,

National Tsing Hua University,
Taiwan

We encourage you to make the most of these sessions and to engage actively in networking with peers and industry experts. The connections you forge here will be instrumental in catalyzing new ideas and collaborations that support your future research and professional success. We anticipate that APCCAS 2025 will be an inspiring and productive milestone, helping to chart the technological direction our community needs in this transformative AI era.

Finally, we extend our profound gratitude to all who made this conference possible: our dedicated Organizing Committee and Technical Program Committee (TPC) members for their countless hours of service; our corporate and institutional sponsors for their generous support; the speakers and attendees who are the lifeblood of this event; IEEE for its continued guidance; and the City of Busan for its gracious hospitality and stunning setting.

We look forward to sharing a successful and impactful conference with you here in vibrant Busan.

Thank you.

MESSAGE FROM TPC CHAIR

On behalf of the Technical Program Committee, it is my great pleasure to welcome you to the IEEE Asia Pacific Conference on Circuits and Systems (APCCAS 2025), which will be held from October 12th to 15th, 2025, at the Paradise Hotel in Busan, Korea.

APCCAS has established itself as a premier regional conference of the IEEE Circuits and Systems Society, bringing together researchers and professionals from around the world to share their latest achievements and insights in circuits and systems.

The theme of APCCAS 2025, "Next-Generation Circuits and Systems from Silicon to Intelligence," reflects the exciting evolution of our field. Circuits and systems are no longer limited to traditional silicon platforms; instead, they are becoming the foundation of intelligent technologies that drive innovations in communications, healthcare, mobility, and sustainable computing. This conference highlights the cutting-edge research and emerging applications that will shape the next generation of circuits and systems.

The APCCAS 2025 technical program features 225 high-quality papers across 31 technical sessions. This includes 178 regular papers presented in 22 oral sessions and 2 poster sessions, as well as 47 special session papers presented in 9 special sessions. These selected papers represent a diverse and competitive set of submissions, reflecting the strong global participation and impact of APCCAS.

We are also delighted to feature 4 keynote speeches from distinguished leaders in academia and industry, as well as 5 tutorials designed to provide educational value to participants at all levels. In addition, new initiatives such as Live Demo Session, PrimeAsia, AutoCAS, and two Industrial Sessions that will bridge academia and industry through real-world perspectives and applications.

I would like to extend my sincere gratitude to all contributors to the technical program, including authors, reviewers, special session organizers, and committee members. Your dedication and effort are the driving force behind the success of APCCAS 2025.

We hope that you will find the technical program both enriching and inspiring, and that APCCAS 2025 will serve as a platform for fruitful discussions, meaningful connections, and future collaborations.

Youngmin Kim

Technical Program Committee Chair, APCCAS 2025

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Atsushi Takahashi *(Institute of Science Tokyo, Japan)*

Neural and Nonlinear Circuits and Systems

Kuduck Kwon (Kangwon National University, Korea)
Hiroo Sekiya (Chiba University, Japan)

TIME TABLE

SUNDAY_ OCTOBER 12, 2025

From	Till	LOBBY 2F	Sydney 2F	Grand Ballroom 2F	Napoli 2F	Venice 2F	Miami 2F	Capri 2F	Sicily 1F
12:00	13:00	On-site Registration							
13:00	14:00		Tutorial 1					Tutorial 4	
14:00	15:00		Tutorial 2						
15:00	16:00		Tutorial 3					Tutorial 5	
18:00	20:00	**Welcome Reception** (Sicily Room 1F)							

MONDAY_ OCTOBER 13, 2025

From	Till	LOBBY 2F	Sydney 1+2 2F	Grand Ballroom 2F	Napoli 2F	Venice 2F	Miami 2F	Capri 2F	Sicily 1F
9:30	10:00	On-site Registration	Sponsor Exhibition / Live Demo; Poster Exhibition (1) **Poster**						
10:00	10:20			**Opening Ceremony** (2F Grand Ballroom)					
10:30	11:20			**Keynote-1 (50mins)** (2F Grand Ballroom)					
11:20	11:30			**Break** (10min.)					
11:30	12:20			**Keynote-2 (50mins)** (2F Grand Ballroom)					
12:20	13:30			**Lunch** (70min.) (2F Grand Ballroom)					Young Professional
13:30	13:45			**Industrial Session 1**	**DI 1** 38	**AM 1** 6	**AI 1** 14	**SS1** 69	**SS2** 17
13:45	14:00				128	112	26	108	42
14:00	14:15				223	234	134	141	121
14:15	14:30				230	263	153	161	137
14:30	14:45				248	290	259	169	245
14:45	15:00			**Break & Poster Standing Exhibition Time (15mins)**					
15:00	15:15				**DI 2** 9	**AM 2** 8	**AI 2** 19	**SS3** 64	**SS4** 15
15:15	15:30				49	32	44	68	16
15:30	15:45				195	154	91	76	28
15:45	16:00				239	193	171	110	133
16:00	16:15				282	291	292	155	249
16:15	16:30			**Break & Poster Standing Exhibition Time (15mins)**					
16:30	16:45					**AM 3** 33	**AI 3** 48	**RF 1** 41	**SS5** 24
16:45	17:00					46	109	104	30
17:00	17:15					113	220	177	45
17:15	17:30					244	262	252	50
17:30	17:45					246	331	297	127
17:45	18:00	Break Time (15min.)							
18:00	20:00	**Banquet** (2F Grand Ballroom)							

TUESDAY_ OCTOBER 14, 2025

From	Till	LOBBY 2F	Sydney 1+2 2F	Grand Ballroom 2F	Napoli 2F	Venice 2F	Miami 2F	Capri 2F	Sicily 1F
9:00	9:15	On-site Registration	Sponsor Exhibition; Poster Exhibition (2) **Poster**		**DI 3** 149	**PE** 95	**AI 4** 22	**SS6** 60	**SS7** 132
9:15	9:30				164	105	65	74	209
9:30	9:45				199	165	190	81	219
9:45	10:00				216	201	217	173	229
10:00	10:15				218	251	222	202	242
10:15	10:30				349	266	293	261	277
10:30	10:40			Break (10min.)					
10:40	11:30			**Keynote-3 (50mins)** (2F Grand Ballroom)					
11:30	12:20			**Keynote-4 (50mins)** (2F Grand Ballroom)					
12:20	13:30			Lunch (70min.) (2F Grand Ballroom)					
13:30	13:45			**AM 4** 18	**RF 2** 83	**AM 5** 129	**BM** 118	**AutoCAS**	**SS8** 21
13:45	14:00			174	125	148	138		54
14:00	14:15			183	241	159	167		299
14:15	14:30			267	273	236	188		304
14:30	14:45			296			276		336
14:45	15:00			**Break & Poster Standing Exhibition Time (15mins)**					
15:00	15:15			**Industrial Session 2**	**CM** 55	**AM 6** 61	**SN** 97	**AutoCAS**	**SS9** 39
15:15	15:30				62	67	283		77
15:30	15:45				85	140	82		124
15:45	16:00				142	156	103		146
16:00	16:15				231	158	237		265
16:15	16:30			**Break & Poster Standing Exhibition Time (15mins)**					
16:30	16:45			**Industrial Session 3**	**DI 4** 98	**AM 7** 11	**AI 5** 106	**AutoCAS**	**Prime Asia** 90
16:45	17:00				135	71	150		301
17:00	17:15				160	93	221		335
17:15	17:30				228	189	253		360
17:30	17:45				281	258	338		363
17:45	18:20	Break Time (25min.)							
18:20	21:00	**Farewell Reception** (Haeundae Byeolbam)							

WEDNESDAY_ OCTOBER 15, 2025								
		LOBBY	Sydney 1+2	Grand Ballroom	Napoli	Venice	Miami	Capri	Sicily
From	Till	2F	2F	2F	2F	2F	2F	2F	1F
10:00	17:00	Committee Meeting & Industry–University–Research Collaboration Roundtable							

Regular Sessions			
DI 1	Advanced Digital Circuit Design	AI 1	Lightweight AI/ML Systems
DI 2	Crypto & Fault-Tolerant Systems	AI 2	AI/ML Accelerators
DI 3	Digital Signal Processing Accelerators	AI 3	AI/ML Algorithms
DI 4	Computation Optimization	AI 4	PIM/CIM Systems
AM 1	Analog and Mixed Signal Systems	AI 5	Emerging AI/ML Solutions
AM 2	SAR ADCs and its Building Blocks	RF 1	High Performance RF/mm-Wave Oscillators
AM 3	Delta-Sigma ADCs and Power Conversion Techniques	RF 2	RF Transceivers and Building Blocks
AM 4	Analog Amplifiers and Filters	PE	Power and Energy Circuits and Systems
AM 5	High-speed Wireline Techniques	BM	Biomedical Circuits and Systems
AM 6	Emerging Computing Systems	CM	Beyond CMOS: Nanoelectronics and Hybrid Systems Integration
AM 7	Sensors and Precision References	SN	Sensory, Neural, and Nonlinear Circuits and Systems

Special Sessions	
SS 1	Advanced RF Transceiver Circuits for Next-Generation Wireless Systems
SS 2	Circuits and Applications for Energy-Efficient Edge Systems
SS 3	Display Driver and Touch Readout Circuits
SS 4	Software-Hardware Co-Design for Neural Networks
SS 5	Next-Generation Circuit Techniques: From Analog and Power to Digital Compute
SS 6	Neural Modeling, AI Techniques, and Nonlinear Circuits in Emerging Technologies (6 papers)
SS 7	Wearable Circuits & Systems for Quality-of-Life: Innovations in GeronCAS (6 papers)
SS 8	Energy-Efficient Hardware Architectures for Advanced Edge Computing Applications
SS 9	Recent Advances and Design Trends in Power Management Ics

TUTORIAL (SUNDAY, October 12)

Tutorial 1

Chair : Prof. Jerald Yoo (Seoul National University, Korea)

13:00~14:00, SUNDAY_OCTOBER 12, 2025
SYDNEY (2F)

Designing compact SoC PWM switched-inductor power supplies

Gabriel A. Rincón-Mora

Motorola Solutions Foundation Professor
School of Electrical and Computer Engineering,Georgia Institute of Technology, USA

Biography

Gabriel A. Rincón-Mora is Motorola Solutions Foundation Professor, Fellow of the National Academy of Inventors, Fellow of the IEEE, and Fellow of the Institution of Engineering and Technology. He was with Texas Instruments in 1994–2004 and has been with the Georgia Institute of Technology since 1999. He's received the IEEE Charles A. Desoer Technical Achievement Award, Distinguished Faculty Achievement Award, IEEE Joseph M. Biedenbach Outstanding Engineering Educator Award, IEEE Outstanding Educator Award, Charles E. Perry Visionary Award, Three-Year Patent Award, National Hispanic in Technology Award, Orgullo Hispano Award, Hispanic Heritage Award, State of California Commendation Certificate, and IEEE Service Award. His body of work includes 4 textbooks, 5 slide books, 3 literary books, 8 handbooks, 4 book chapters, 44 patents, over 200 articles, over 26 commercial power-chip products released to production, 25 educational videos, and over 170 keynote addresses, distinguished lectures, and research seminars.

Abstract

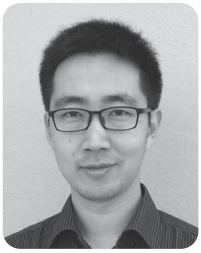
Switched-inductor power supplies are pervasive in electronics. This is because they deliver a large fraction of the power they draw from the input source with an output current or voltage that is largely independent of the load. Keeping the output current or voltage steady this way is ultimately the responsibility of the feedback controller. This talk uses insight and intuition to show how SoC pulse-width-modulated (PWM) loops switch the inductor and offset the current or voltage they control. The presentation reviews the feedback response of switched inductors and discusses how PWM loops operate, control, and offset the current or voltage they regulate. The material covers current and voltage loops, current-mode voltage loops, load-dump response and compensation, and compact SoC contractions.

Tutorial 2

Chair : Prof. Jerald Yoo (Seoul National University, Korea)

14:00 ~ 15:00, SUNDAY, OCTOBER 12, 2025
SYDNEY (2F)

Overcoming the Transimpedance Limit: On the Design of Low-Noise TIA



Dan Li
Professor
School of Microelectronics, Xi'an Jiaotong University, China

Biography

Dan Li received the B.E. and M.E. degrees from Northwestern Polytechnical University, Xi'an, in 2004 and 2007, respectively, and the Ph.D. degree from the University of Pavia, Pavia, Italy, in 2013. From 2007 to 2009, he worked at the Nvidia Shanghai R&D Center, where he focused on custom SRAM circuit design. From 2011 to 2014, he was with the Studio di Microelettronica, STMicroelectronics, Pavia, Italy, working on CMOS optical receivers for 100 GbE optical links and silicon photonics applications. He joined Xi'an Jiaotong University, Xi'an, in 2015, where he currently serves as a professor. His current research interests include high-speed optical interconnects, 3D sensing, and low-power mixed-signal circuits. He has served as Track Chair (Wireline) and TPC Member of IEEE ICTA, Publicity Chair of IEEE ICECS 2020, Sponsorship/ Exhibition Chair of IEEE ICTA 2022, and Local Arrangement Chair of IEEE BioCAS 2024.

Abstract

With the mass deployment of optical links to meet the ever-increasing communication bandwidth demands from data communication and AI, there is a growing need for low-cost components. Furthermore, the advent of Co-Packaged Optics (CPO)—where electronics and photonics are integrated into a single package—will further drive improvements in bandwidth density and power efficiency. In this context, integrated solutions are not only desirable but often essential, leading to the adoption of silicon photonics and CMOS-based electronics, replacing the traditional dominance of III-V optics and SiGe electronics.

While CMOS is optimized for large-scale, digital-intensive functions, it has inherent weaknesses in high-speed analog performance. This tutorial addresses the design challenges in CMOS optical receiver (Rx) front-ends, with a particular focus on low noise. Noise is one of the most critical factors determining receiver performance and remains the most challenging aspect of Rx design. This is largely constrained by the relatively poor performance of CMOS transistors in terms of transconductance, gain, breakdown voltage, and linearity—limiting their use in broader scenarios such as long-reach and high-modulation applications.

To address this, the concept of “overcoming the transimpedance limit” is introduced as the underlying principle for low-noise receiver design. Under this methodology, two approaches are presented as toolkits for low-noise transimpedance amplifier (TIA) design: Type I (Breaking the Transimpedance Limit) and Type II (Exceeding the Transimpedance Limit). Design examples across various electronic and photonic technologies will be provided to guide the audience at both conceptual and practical levels. This tutorial helps researchers, students, and practitioners grasp the fundamentals of and gain insights into designing optical transceivers, silicon photonics systems, wireline communications, and high-speed electronics.

Tutorial 3

Chair : Prof. Seungkyu Choi (Kyung Hee University, Korea)

15:00 ~ 16:00, SUNDAY, OCTOBER 12, 2025
SYDNEY (2F)

Short-Length ECC Decoders: Design Challenges for Future URLLC Systems

Youngjoo Lee
Associate Professor
Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Korea

Biography

Youngjoo Lee received the B.S., M.S., and Ph.D. degrees in Electrical Engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2008, 2010, and 2014, respectively.

Since 2025, he has been with the School of Electrical Engineering at KAIST, where he is currently an Associate Professor. Prior to joining KAIST, he was with the Interuniversity Microelectronics Center (IMEC), Leuven, Belgium, from 2014 to 2015, where he worked on reconfigurable SoC platforms for software-defined radio systems. He was an Assistant Professor in the Department of Electronic Engineering at Kwangwoon University, Seoul, South Korea, from 2015 to 2017. From 2017 to 2025, he served as a faculty member in the Department of Electrical Engineering at Pohang University of Science and Technology (POSTECH), Pohang, South Korea.

His current research interests include algorithm-hardware co-design for application-specific processors, energy-efficient machine learning accelerators, advanced error correction codes, and next-generation wireless systems.

More information is available at: https://sites.google.com/view/epiclab

Abstract

As 5G advances and 6G approaches, ultra reliable low latency communication (URLLC) is becoming increasingly important in next generation wireless systems. The growing presence of intelligent applications such as autonomous systems, real time control, and on device AI has led to a rapid increase in the demand for fast and reliable transmission of short data packets. This shift brings new and significant challenges to error correction coding, especially in terms of decoding performance, latency, throughput, and energy efficiency.

Short length ECC decoders, unlike those designed for longer codes, face unique design constraints due to limited redundancy and tighter timing requirements. Traditional approaches are often insufficient in these scenarios. In this tutorial, we will examine the key challenges in designing ECC decoders for URLLC applications using short codes. We will first explore how existing polar decoders, currently used in 5G systems, can be optimized for improved performance in short packet communication. In addition, we will discuss emerging ECC schemes that aim to replace the current 5G polar codes. We will highlight important considerations in decoder implementation for these new codes and compare their strengths and weaknesses against standard polar decoders

Tutorial 4

Chair : Prof. Junghyup Lee (Daegu Gyeongbuk Institute of Science and Technology, Korea)

13:00 ~ 15:00, SUNDAY, OCTOBER 12, 2025
CAPRI (2F)

Advanced Techniques for High Efficiency Oversampling Data Converters from Discrete-Time to Continuous-Time: Fundamentals, Recent Trends, and Perspectives

Sai-Weng Sin, Terry

Professor
Faculty of Science and Technology, University of Macau, Macao, China

Biography

Sai-Weng Sin is currently a Professor with the Dept. of ECE, Faculty of Science and Technology, and the Deputy Director (Academic) of the Institute of Microelectronics, as well as the Deputy Director of State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau.

Dr. Sin is currently serving as the Associate Editor-in-Chief (Digital Communications) of the IEEE Transactions on Circuits and Systems II – Express Briefs, and the chair of the data converter subcommittee in the IEEE Custom Integrated Circuits Conference (CICC). He is/has been members of the Technical Program Committee of the IEEE Symposium of VLSI Circuits (VLSI), IEEE Asian Solid-State Circuits Conference (A-SSCC), International Symposium on Circuits and Systems (ISCAS), Int. Conference on Integrated Circuits, Technologies and Applications (ICTA), and Associate Editors of Journal of Semiconductor and IEEE Access, and Guest Editor of IEEE Open Journal of Solid-State Circuits Society (OJ-SSCS). He is a Distinguished Lecturer of IEEE Solid-State Circuits Society from 2024 to 2025. He was the co-recipient of the 2011 ISSCC Silk Road Award and the 2011 State Science and Technology Progress Award (second-class), China.

Liang Qi

Associate Professor
School of Integrated Circuits, Shanghai Jiao Tong University, China

Biography

Liang Qi (Senior Member, IEEE) received B.Sc. degree from Xidian University, China, in 2012 and Ph.D. degree from University of Macau, Macao, China, in 2019.

He currently works as an Associate Professor with the School of Integrated Circuits, Shanghai Jiao Tong University (SJTU). Before he joined SJTU, he worked with Shanghai Hisilicon, where he conducted the project of multi-band (2G-5G) RX ADC. He was a Visiting Scholar at Ulm University, Germany, during the Ph.D. studies. His research interests include high-performance data converters and analog mixed-signal integrated circuits.

Dr. Qi has served as an Associate Editor for the IEEE Transactions on Circuits and Systems II – Express Briefs and the Integrated Circuits and Systems (ICAS) journal. He also is/has been a TPC Member for IEEE APCCAS, ICSICT, ICTA, and ASICON. He received Macao Scientific and Technology Research and Development for Postgraduate Award in 2016 and Outstanding Young Scholar Paper Award in IEEE ASICON 2021, respectively.

Abstract

High efficiency oversampling data converters have become increasingly popular and significant in the various emerging applications, ranging from the data acquisition in IoT sensor nodes that demands an ultra-high resolution with very low power consumption to wideband wireless communications in medium/high resolution.

Part-I: Incremental ADCs (IADCs) play a vital role in modern applications, from high-end audio to IoT sensors. Significant advances in recent years have enhanced high-resolution IADC design, particularly in managing critical issues like thermal noise and DAC mismatches. This part provides a thorough examination of various design strategies within IADCs. It explores how weighting affects noise and mismatch performance, explains its role in algorithms, and presents cutting-edge architectures derived from academic research. Concrete design examples demonstrate these concepts in practice.

Part-II: Due to the resistive inputs and implicit anti-aliasing filtering, continuous-time (CT) delta-sigma ADCs (DS-ADCs) are favorable for wireless applications. The maximum clock frequency of CT DS-ADCs has increased significantly over the past decade. This trend results from advances in CMOS technologies and innovative ways to use this technology. This part covers the background and recent architectural and circuit innovations regarding CT DS-ADCs. Moreover, state-of-the-art examples will be presented as well as the future perspectives.

Tutorial 5

Chair : Prof. Junghyup Lee (Daegu Gyeongbuk Institute of Science and Technology, Korea)

15:00 ~ 16:00, SUNDAY, OCTOBER 12, 2025
CAPRI (2F)

SPAD-Based Solid-State LiDAR in CMOS: From Fundamentals to State-of-the-Art Integration

Seong-Jin Kim
Associate Professor
Department of System Semiconductor Engineering, Sogang University, Korea

Biography

Seong-Jin Kim received his B.S. degree in electrical engineering from the Pohang University of Science and Technology, Pohang, South Korea, in 2001, and M.S. and Ph.D. degrees in electrical engineering from KAIST, Daejeon, South Korea, in 2003 and 2008, respectively.

From 2008 to 2012, he was a Research Staff Member at the Samsung Advanced Institute of Technology, Yongin, South Korea, where he was involved in the development of CMOS imagers for real-time acquisition of 3-D images. From 2012 to 2015, he was with the Institute of Microelectronics, A*STAR, Singapore, where he was involved in the design of analog-mixed signal circuits for various sensing systems. From 2015 to 2024, he was an Associate Professor at the Ulsan National Institute of Science and Technology, Ulsan, South Korea. In 2024, he joined Sogang University, Seoul, South Korea, as an Associate Professor. He is a co-founder of SolidVue, a LiDAR startup company in South Korea. His current research interests include high-performance imaging devices, LiDAR systems, and biomedical interface circuits and systems.

Dr. Kim has served on the Technical Program Committee at the IEEE International Solid-State Circuits Conference (ISSCC) from 2019 to 2024 and was the Country Representative of South Korea for the ISSCC Far-East Region in 2021. He was a co-recipient of the IEEE ISSCC Silkroad Awards in 2020 and 2021.

Abstract

This tutorial will present a comprehensive overview of the enabling technologies behind single-photon avalanche diode (SPAD)-based solid-state CMOS LiDAR sensors that have emerged as a key component in autonomous vehicles and immersive mobile applications such as augmented and virtual realities (AR/VR). It will begin with an introduction to the fundamental principles of both direct and indirect time-of-flight (ToF) techniques. Subsequently, the tutorial will delve into the three core building blocks of a SPAD-based LiDAR system: (1) SPAD devices and analog front-end circuit to enable photon-level sensitivity; (2) time-to-digital converters (TDC) to translate photon arrival times into precise temporal measurements; and (3) histogram-based signal processing units to reconstruct depth information from stochastic photon detections. The session will finally explore recent advances in fully integrated on-chip histogramming TDC architectures, highlighting selected state-of-the-art implementations.

OPENING CEREMONY (MONDAY, OCTOBER 13)

10:00~10:20 MONDAY, OCTOBER 13, 2025
GRANDBALL ROOM (2F)

Welcome Address

Kyung Ki Kim
General Chair
(Daegu University, Korea)

Conference Statistics

Youngmin Kim
Technical Program Chair
(Hongik University, Korea)

Announcements

Youngmin Kim
Technical Program Chair
(Hongik University, Korea)

Keynote Speeches (MONDAY, OCTOBER 13)

Keynote Speech 1

10:30 ~ 11:20, MONDAY_OCTOBER 13, 2025

Grand Ballroom(2F)

Exynos On-device AI

Hyukjune Chung

Corporate EVP / Head of AP Development
System LSI, Samsung Electronics Co., Ltd., Korea

Biography

2020 – Current: Samsung Electronics
Current position – Head of AP Development
Experiences in leading SOC development, SOC architecture design

2005 – 2020: Qualcomm
Experiences in low power architecture & system design, video/computer vision HW/SW & architecture design, Mobile / Visual standard engineering & delegation including MPEG, JVT, 3GPP, 3GPP2.

Ph.D. University of Southern California, Department of Electrical Engineering, 2004
M.S. Seoul National University, School of Electrical Engineering, 1999
B.S. Seoul National University, School of Electrical Engineering, 1997

Abstract

In this talk, I will focus on on-device AI computing, and for this, I will present evolution of Exynos AI HW/SW solutions, challenges to support generative AI processing, and systematic approaches to overcome these challenges.

Keynote Speech 2

11:30 ~ 12:20 MONDAY_OCTOBER 13, 2025

Grand Ballroom(2F)

Silicon to Systems 2035: Re-Engineering Engineering for an AI-Driven World

Frank Schirrmeister

Executive Director
Strategic Programs, System Design, Synopsys, USA

Biography

Frank Schirrmeister is Executive Director, Strategic Programs, System Solutions in Synopsys' Products & Markets Group. He leads strategic activities across system software and hardware assisted development for industries like automotive, data center and 5G/6G communications, as well as for horizontals like Artificial Intelligence / Machine Learning. Prior to Synopsys, Frank held various senior leadership positions at Arteris, Cadence Design Systems, Imperas, Chipvision, and SICAN Microelectronics, focusing on product marketing and management, solutions, strategic ecosystem partner initiatives, and customer engagement. He holds an MSEE from the Technical University of Berlin and actively participates in cross-industry initiatives as Engineering Program Chair at the ACM/IEEE Design Automation Conference.

Abstract

By 2035, our world will be shaped by intelligent systems built upon semiconductor chips and systems of unimaginable complexity. These capabilities will redefine our day-to-day life from healthcare to transportation, but their creation demands a fundamental shift in how we design and engineer them. This presentation will present an outlook on the future of chip and system design, addressing the central question: How must we re-engineer engineering itself to meet the challenges of the next decade and beyond?

The presentation will explore the forces shaping the silicon of 2035, from the dominance of software, semiconductor hardware complexity, to the intricacies chip architectures as the industry is pushing the boundaries of processing, memory and interconnect. A key focus will be the dual inflection point of Artificial Intelligence—both as the primary workload driving performance requirements for advanced computing from data centers to edges and as the essential tool for mastering development, verification, validation and implementation complexity of semiconductor devices. Extrapolating lessons from the past decade and insights from industry leaders, this presentation will identify the primary challenges facing our design flows, methodologies, and the engineering workforce.

As an outlook for the semiconductor, systems and design automation space, this talk will discuss the necessary evolution of our tools and processes to enable the development of these advanced systems, providing a strategic perspective on how we can collectively build and distribute that future.

Keynote Speeches (TUESDAY, OCTOBER 14)

Keynote Speech 3

10:40~11:30, TUESDAY_OCTOBER 14, 2025
Grand Ballroom(2F)

The Next-Generation AI Accelerator: Redefining Inference for a Sustainable AI Future

Youngjin Cho
Vice President, Head of Hardware
Hardware Development, FuriosaAI, Korea

Biography

Youngjin Cho is Vice President of Hardware at FuriosaAI, where he leads the development of SoCs and AI accelerators. Previously, he spent 16 years at Samsung Electronics, serving as Corporate Vice President and leading SSD controller programs and ASIC/SoC architecture. He was a Visiting Scholar at Stanford University in 2017 and holds a Ph.D. in Computer Science from Seoul National University in 2009. His deep expertise in system architecture and silicon design now drives FuriosaAI's next-generation AI inference chip development.

Abstract

As AI inference becomes ubiquitous infrastructure, the industry faces critical challenges in achieving sustainable and cost-effective computing. Current GPU-based solutions, not purpose-built for inference, suffer from poor energy efficiency that threatens AI scalability. This keynote presents TCP (Tensor Contraction Processor), a domain-specific architecture that elevates tensor contraction as the primitive operation. By introducing low-level einsum notation with explicit memory layout and scheduling, TCP enables unprecedented flexibility through software-defined topology and automated compilation, while achieving optimal performance. Our silicon implementation RNGD delivers 512 TFLOPS (FP8) at 150W TDP for air-cooled data centers, demonstrating 4.1× better first token latency and 2.7× improved throughput/watt on LLaMA-7B versus GPUs. This presentation will share our journey from concept to commercial deployment, examining how domain-specific design choices enable sustainable AI infrastructure.

Keynote Speech 4

11:30~12:20, TUESDAY_OCTOBER 14, 2025

Grand Ballroom(2F)

The Roadmap to the Future of Computing: Quantum-Centric Supercomputing

Hanhee Paik

Director, Quantum Algorithms Centers and Quantum-HPC Partnerships, IBM, USA

Biography

Dr. Hanhee Paik is the Head of IBM Quantum Japan and a Senior Research Scientist at IBM Quantum. Her research career has been focused on understanding the coherence mechanisms of superconducting qubits and developing superconducting multi qubit architectures. Dr. Paik pioneered the novel design of a supercond ucting qubit that helped the industry push the quality of quantum computing performance, greatly impacting the quantum computing community. Today's IBM Quantum systems' coherence times benefit from Dr. Paik's work. She played a pivotal role developing IBM Quantum's 16 qubit processors. Over the last few years, she has turned her focus to IBM Quantum's efforts to develop the global quantum ecosystem. Dr. Paik was elected an American Physical Society Fellow in 2021 for pioneering a novel superconducting qub it architecture that catalyzed the commercialization of superconducting quantum computing, and contributing to the advancement quantum computing research in the industry

Abstract

As classical computing nears its limits, quantum computing offers a transformative paradigm for tackling the most complex scientific and engineering challenges. This keynote presents IBM's roadmap and vision for advancing quantum technology to usher in the era of Quantum-Centric Supercomputing.

The presentation will focus on the continuous evolution of superconducting qubit architectures, a field Dr. Paik pioneered. We'll detail the strategy for achieving utility-scale quantum systems by emphas

Young Professional (MONDAY, OCTOBER 13)

Young Professional 1

12:20~12:45, MONDAY_OCTOBER 13, 2025

SICILY (1F)

Chair : Prof. Sunmean Kim (Kyungpook National University, Korea)

Handle with care: how to bring research outputs in the field of electronics and neuromorphics from the lab to the bedside, without hurting someone in the process

Jacopo Secco

Co-Founder and COO, Omnidermal Biomedics
Assistant Professor, Politecnico di Torino, Italy

Biography

Jacopo Secco, Ph.D. in Engineering and MBA, is Assistant Professor at Politecnico di Torino, where he founded the NEURICA Lab to bridge academia and industry. His group develops medical devices for wound care, neurorehabilitation, and advanced computing techniques. As co-founder of Omnidermal Biomedics, he led the creation of AI-powered solutions such as Wound Viewer and certified ventilators, combining research, innovation, and entrepreneurship.

Abstract

The journey from laboratory discovery to clinical application is filled with both opportunity and risk. In the field of electronics and neuromorphic engineering, the potential to create transformative healthcare technologies is immense, but so are the challenges of ensuring safety, efficacy, and societal acceptance. In this talk, I will share insights from my dual path as academic researcher and entrepreneur: from developing memristor-based neuromorphic circuits to co-founding a medical device company that introduced Wound Viewer, the first AI-powered telemedicine system for chronic wound care, and rapidly delivering certified ventilators during the COVID-19 crisis. These experiences highlight the tension between scientific ambition, regulatory rigor, and business pragmatism. By retracing successes and setbacks, I aim to provide practical advice for young researchers and innovators on how to responsibly transfer knowledge from bench to bedside, embracing entrepreneurship without losing sight of ethics, patient safety, and the long-term sustainability of innovation.

Young Professional 2

12:45~13:10, MONDAY_OCTOBER 13, 2025

SICILY (1F)

Chair : Prof. Sunmean Kim (Kyungpook National University, Korea)

Neural Network Data Compression Method Using Huffman Coding and High-Throughput Decompression Hardware Architecture

Injae Yoo

Associate Professor, School of Electrical & Electronics Engineering, Pusan National University, South Korea

Biography

Injae Yoo is an Associate Professor at Pusan National University's School of Electrical and Electronics Engineering. He received his bachelor's, master's, and doctoral degrees in electrical engineering from KAIST in South Korea between 2011 and 2017. After graduation, he spent a year as a Senior Engineer at SK Hynix before moving to Silicon Valley in 2018 to join Marvell Technology. During his four years at Marvell, he advanced through several roles and led the development of data-path designs for high-speed PCIe 5.0 SSD controllers. In 2022, he transitioned to Google, where he contributed to edge TPU design for Google's mobile Tensor processors for two years. His research interests include hardware accelerators for deep neural networks, error-correcting codec hardware, and data storage solutions.

Abstract

With generative AI models growing exponentially, there is growing focus on methods to reduce data movement between memory and AI accelerators by compressing neural network parameters in DRAM. However, this approach requires on-chip decompression circuits, presenting two key challenges. First, to offset the area and power consumption of additional circuits, flexible compression algorithms and hardware architectures must effectively compress both parameters and activations. Second, extremely fast decompression hardware matching DRAM bandwidth speeds is essential for real-time operation. This talk presents a Huffman coding-based lossless compression method for neural network parameters and activations, along with a high-throughput decompression hardware architecture that addresses these challenges.

AutoCAS (Autonomous Mobility CAS, TUESDAY, OCTOBER 14)

13:30~17:45 TUESDAY, OCTOBER 14, 2025
CAPRI ROOM (2F)

Chair : Prof. Jusung Kim (Ewha Womans University, Korea)

13:30~13:40	**Welcome Address**
	Jusung Kim General Chair (Ewha Womans University, Korea)
13:40~14:20	**Enhancing Autonomous Mobility with Vision-Language-Action World Models**
	Yubeen Park Managing Director (MAUM.AI, Korea)
14:20~15:00	**Overview of 3D Sensor Technologies for Autonomous Driving**
	Max Kim Principle System Engineer (Samsung Semiconductor, USA)
15:00~15:40	**Semiconductor Competitiveness: The Key to Capturing the Automotive AI Market—What Matters Most**
	Kyoungmook Lim CTO (BOS Semiconductors, Korea)
15:40~16:10	**Break**
16:10~16:40	**Battery Management Systems for EVs and Energy Storage**
	Krishna Kanth Avalur Founder and CTO (MOSart Labs, India)
16:40~17:40	**Panel Discussion(The Rise of AI Edge & Connected Electronics for Automotive)**
	- Edge AI, cloud connectivity, and real-time processing are transforming automotive industry - Security of electronic products in automotive - Safety requirements for automotive 1) *Moderator - Preet Yadav, Chair IEEE CASS Delhi Chapter, Head India Innovation Ecosystem, NXP Semiconductors, India* 2) *Dr. Krishna Kanth Avalur, Founder & CTO, MOSart Labs, India* 3) *Yubeen Park Managing Director (MAUM.AI, Korea)* 4) *Max Kim Principle System Engineer (Samsung Semiconductor, USA)* 5) *Kyoungmook Lim CTO (BOS Semiconductors, Korea)*
17:40~17:45	**Farewell**

Industrial Session 1 (MONDAY, OCTOBER 13)

IN1 PIM, LLM, and the On-device AI Chip Revolution

Chair : Min-Seong Choo (Hanyang University, Korea)

13:30~14:45, MONDAY_ OCTOBER 13, 2025

Grand Ballroom (2F)

IN1-1 13:30-14:05

PIM moves forward to accelerate LLM

Jaehyun Park

Staff Engineer, Samsung Electronics

Abstract

Large language models (LLMs) have transformed modern applications but demand unprecedented computing resources, particularly large memory capacity and high bandwidth for weight processing. While logic process technology has advanced rapidly, memory process scaling has lagged behind, creating a performance bottleneck where LLM decode execution is constrained by memory. To address this, Samsung introduced breakthrough processing-in-memory (PIM) solutions that significantly enhance main memory bandwidth. Using a high-bandwidth GPU cluster with an HBM-PIM system and an LPDDR5-PIM–based system, transformer-based LLMs achieved performance improvements of up to 1.93× and 2.73×, respectively.

IN1-2 14:05-14:40

The On-device AI Chip Revolution

Jay(Jeongwook) Kim
EVP, DeepX, Korea

Abstract

We are entering the era of "AI Everywhere," where Artificial Intelligence (AI) is becoming a foundational technology for society, much like electricity or Wi-Fi. AI is evolving beyond a mere tool that offers convenience into "Ambient Intelligence," deeply integrated and interacting within our daily lives and industrial ecosystems. Amidst this paradigm shift, NPUs (Neural Processing Units), which process vast AI computations in real-time, are no longer an option but have become an indispensable component, akin to the very heart of future technology.

Until now, most AI services have been delivered by relying on cloud servers with immense computing resources. While this model contributed to the initial proliferation of AI technology, it is simultaneously revealing clear technical and structural limitations. Concerns over data security and privacy breaches, which arise from transmitting sensitive data to central servers, are eroding public trust in the technology. Network latency, caused by physical distance, acts as a critical drawback in fields like autonomous driving and robotics where split-second decisions are paramount. Furthermore, the massive operational costs required to transmit and process data from billions of devices to the cloud are becoming a major barrier to the widespread adoption and democratization of AI services.

To realize the true potential of automation, hyper-personalization, and real-time intelligent services, a new paradigm that moves beyond the centralized model is urgently needed.

The fundamental solution lies in On-Device AI. This is a technology that embeds the "brain" of AI directly onto the device where data is generated and consumed, enabling it to infer and make decisions independently without a network connection. By bypassing the cloud, On-Device AI innovatively solves the persistent challenges of cost, security, and speed. Data remains on the user's device, ensuring complete privacy protection; it guarantees instantaneous responsiveness with zero physical latency; and it maximizes the economic viability of AI technology by eliminating unnecessary data transmission costs.

At this major inflection point, as the global AI market shifts from the cloud to the device, we at DeepX are confident in the infinite potential of the exponentially growing On-Device AI market. We are not merely following this trend; rather, we aim to lead this massive transformation through our core technologies and become a key player in pioneering this new era

Industrial Session 2 (TUESDAY, OCTOBER 14)

IN2 Emerging Sensor Technologies for Physical AI

Chair : Young-Ha Hwang (Soongsil University, Korea)

15:00~16:15, TUESDAY_ OCTOBER 14, 2025

Grand Ballroom (2F)

IN2-1 15:00-15:18

Printed Deformable Electronic Devices for Practical Uses

Prof. Unyong Jeong

POSTECH/MiDAS H&T

Abstract

Tactile sensors have taking increasing attention for the use in wearable healthcare devices and electronic skins for robots. In fabrication of the deformable tactile sensors, there have been two approaches; electronic sensor and iontronic sensor. Electronic tactile sensors monitor the electrical changes (resistance, capacitance, inductance, voltage, current) resulting from temperature change and mechanical deformation, either with/without selectors (diodes, transistors) and signal modulators (ring oscillator, analog-to-digital converter). Iontronic tactile sensors detect the electrical changes (voltage, capacitance, current) caused by charge distribution and ion transport in an electrolyte-containing medium, either with or without synaptic units used for signal modulation. In both approaches, several technological trends are emerging and competing; time-division multiple access (TDMA) versus event-driven parallel collection, passive sensing versus active sensing, and having multifunctions with clear decoupling between the functions. In this talk, I discuss some of the achievements in both the electronic and iontronic tactile sensors and compare the pros and cons of the approaches in the type of data collection, power supply, structural simplicity, and multifunctionality.

IN2-2 15:19-15:37

Tactile Sensing for Advanced Automation

Dr. Alexander Schmitz
XELA Robotics

Abstract

XELA provides the human sense of touch to robots. Our "uSkin" tactile sensors enable robots to perform tasks that previously only humans could do, like gently grasping or inserting objects, e.g. in assembly or warehouse automation. uSkin is small and easy to integrate into existing grippers and robot hands. The company started in August 2018 as a spin-off from Waseda University and has already >50 customers. The uSkin sensor is a 3-axis tactile sensor module with a soft surface. The uSkin "patch" sensor is available in 5 sizes. uSkin Curved has a curved shape similar to a human fingertip. uSkin Multi-Bend can be bent to attach the sensor to curved objects. We also integrate our sensors in robot hands and grippers. The robot hand has 368 tri-axis sensors. We can also modify uSkin to suit your needs.

IN2-3 15:38-15:56

Edge AI starts in the sensor

Dr. Mustahsin Adib
AMS Osram

Abstract

Industrial AI promises efficiency, automation, and scalability, but its success is fundamentally constrained by the quality and intelligence of the sensors feeding it. While the AI market is expanding rapidly, the sensor market evolves at a different pace—creating a gap between AI's potential and the realities of data collection. Traditional sensors act as passive data sources, often producing redundant or noisy streams that overload AI systems with resource-intensive preprocessing and validation tasks. The complexity lies in bridging this gap: industrial environments demand robust, efficient, and reliable data flows, yet testing, validation, and calibration grow more challenging as sensors integrate AI-like intelligence. The resolution is a new generation of AI-ready sensors that preprocess, compress, and filter information at the edge—reducing energy, latency, and computational costs. This talk will outline the implementation challenge, ams-OSRAM's approach and a call for action for the sensor industry.

IN2-4 15:57-16:15

Metaphotonics-Enhanced CMOS Image Sensor: The Future of Imaging and Sensing

Dr. Radwan Siddique

Samsung Semiconductor, Inc.

Abstract

The CMOS image sensor (CIS) market is rapidly expanding, driven by demand for smaller, smarter, and more capable imaging systems across mobile, automotive, industrial, and AI vision applications. As CIS faces growing challenges in pixel miniaturization, performance and functionality, metaphotonics - nanoscale photonic structures integrated directly on-chip offers a transformative path forward. This talk will introduce the role of metaphotonics-enhanced CIS, showing how it enables performance gains, supports higher pixel resolution, and enhances AI vision capabilities. Examples will highlight how metaphotonics improves light control, reduce crosstalk, and enable new features like spectral tuning and polarization detection on-chip. By co-embedding optical-electrical intelligence at the pixel level, metaphotonics is redefining CIS from imaging devices to multifunctional sensing platforms

Industrial Session 3 (MONDAY, OCTOBER 14)

IN3 **End-to-End Optimization for AI Systems: LLM Efficiency and Chip-to-System Co-Design**

Chair : Min-Seong Choo (Hanyang University, Korea)

16:30~17:45, TUESDAY_ OCTOBER 14, 2025

Grand Ballroom (2F)

IN3-1 16:30-17:05

End-to-End Optimization for Efficient LLM Inference: From Model Compression to Hardware Architecture

Gunho Park

Research Scientist, AI Computing Solution (NAVER Cloud), Korea

Abstract

Large language models deliver impressive capabilities but at high cost in memory traffic, compute, and latency. We present an end-to-end approach to efficient LLM inference that begins with model-compression algorithms and extends through CUDA kernels, runtime policy, and hardware architecture. On the algorithmic side, we revisit quantization beyond fixed-bit settings and introduce formats that enable multi-precision operation with minimal accuracy loss. These choices co-design with custom CUDA kernels to reduce latency and support dynamic, per-request precision selection with negligible overhead. We then map the resulting compute and bandwidth profiles onto custom hardware to fully realize efficiency. Case studies on production-scale LLMs show gains in tokens-per-second and energy efficiency, alongside reductions in memory footprint and total cost of ownership. The result is a practical recipe that links compression decisions to kernel behavior and, ultimately, to architectural implications—enabling consistent, deployable improvements.

IN3-2 17:05-17:40

Digital Twin-Driven Chip-to-System Co-Design

Tai SiK Yang

Professional, LG Electronics CTO SoC R&D Center

Abstract

This presentation introduces a digital twin-based chip-to-system co-design approach for optimizing high-speed interfaces in AI systems. By enabling performance and cost optimization at the design stage, the methodology reduces design iterations and accelerates product development, supporting efficient and timely delivery of AI solutions.

Regular Sessions (MONDAY, OCTOBER 13)

Samsung Electronics Session

DI1 Advanced Digital Circuit Design

Chair: Dong-Jin Chang (Chungnam National University, Korea)

13:30~14:45, MONDAY_ OCTOBER 13, 2025

NAPOLI (2F)

DI1-1 (38)
13:30-13:45

On the Data Dependency of the Read Speed of Low-Voltage SRAM with VSS-Assist Circuitry

Chien-Tung Liu, Yu-Chuan Hou, Tay-Jyi Lin, and Jinn-Shyan Wang
Chung-Cheng University, Taiwan

DI1-2 (128)
13:45-14:00

Via-Configurable Routing Network and Hard Macro Adaptability for 28 nm Structured ASIC

Junyu Lin[1], Binxu Ning[2], Jian Yu[1,2], Ning Chen[1,2], Tianqin Ye[1], and Lei Shen[1,2]
[1]*Fudan University, China*
[2]*Shanghai Fudan Microelectronics Group Co., Ltd., China*

DI1-3 (223)
14:00-14:15

Timing Modeling and Optimization of Ternary Logic Gates for Circuit-level Analysis

Minhyuk Kweon[1], Jeyeong Park[1], Seunghan Baek[2], Seokhyeong Kang[1], and Sunmean Kim[3]
[1]*Pohang University of Science and Technology, Korea*
[2]*Samsung Electronics, Korea*
[3]*Kyungpook National University, Korea*

DI1-4 (230)
14:15-14:30

A Wide-Range Standard-Cell-Compatible Voltage Level Shifter with Transition-Controlled Current Generator in 3-nm Nano-Sheet Technology

Anuj Bhardwaj
ARM Embedded Technologies Pvt Ltd, India

DI1-5 (248)
14:30-14:45

Monolithic Hybrid-3D Standard Cell Library with Sandwiched Inter-Metal Layer for 3D Digital Computation-in-Memory Circuits

Chieh-Ling Lee[1], Chu-Hsiu Hsu[1], Chih-Chao Yang[2], Chang-Hong Shen[2], Kuan-Neng Chen[1], Po-Tsang Huang[1], and Chenming Hu[1,3]
[1]National Yang Ming Chiao Tung University, Taiwan
[2]Taiwan Semiconductor Research Institute, Taiwan
[3]University of California, USA

Synopsys Session

AM1 Analog and Mixed Signal Systems

Chair: Hanwool Jeong (Yonsei University, Korea)

13:30~14:45, MONDAY_ OCTOBER 13, 2025
VENICE (2F)

AM1-1 (6)
13:30-13:45

Power Amplifier-Voltage Cotrolled Oscillator with Mixer for Millimeter-Wave Transmitter Linearization

Wen-Cheng Lai
Ming Chi University of Technology, Taiwan

AM1-2 (112)
13:45-14:00

A Single-Channel 1-GS/s 62.2-dB SNDR Hybrid Voltage-Time Pipelined ADC with Parallel Conversion Technique in 40-nm CMOS

Huilin Zhou, Xinsheng Wang, Congyi Zhang, and Chenrui Liang
Harbin Institute of Technology, China

AM1-3 (234)
14:00-14:15

A Sub-100 nW Power-on-Reset Circuit With Integrated Brown-Out Detection and Autonomous Power Gating for Edge Devices

Inseo Son, Yoochang Kim, and Young-Ha Hwang
Soongsil University, Korea

AM1-4 (263)
14:15-14:30

An Ultra-Low Jitter Divider-Less Phase-Locked Loop using Differential Dual-Edge Sub-Sampling Phase Detector

Anshul Verma[1], and Bishnu Prasad Das[2]
Indian Institute of Technology Roorkee, India

AM1-5 (290)
14:30-14:45

An Analog-Front-End with ultra low-power in optical sensor for FMCW LiDAR system

Yehyeon An, Jonghyun Kim, Seungju Lee, and Jinwook Burm
Sogang University, Korea

ETRI Session

AI1 Lightweight AI/ML Systems

Chair: Seungsik Moon (Chungbuk National University, Korea)

13:30~14:45, MONDAY_ OCTOBER 13, 2025

MIAMI (2F)

AI1-1 (14)
13:30-13:45

FRIEREN: A Lightweight System for Face Resizing Image Detail Quality Evaluation via Robust Estimation of Image Naturalness

Yuan-Kang Lee, Kuan-Lin Chen, and Jian-Jiun Ding
National Taiwan University, Taiwan

AI1-2 (26)
13:45-14:00

Closit: Clipped-Regime Posit Quantization for Edge-Friendly Vision Transformers

Sungsoo Han, Dahun Choi, and Hyun Kim
Seoul National University of Science and Technology, Korea

AI1-3 (134)
14:00-14:15

AxAdderNet: Combining Approximate Computing to Quantized AdderNet

DaeRyong Shin[1], Min Kee Chang[1], HyunJin Kim[1], and Alberto A. del Barrio[2]
[1]Dankook University, Korea
[2]Complutense University of Madrid, Spain

AI1-4 (153)
14:15-14:30

StripDet: Strip Attention-Based Lightweight 3D Object Detection from Point Cloud

Weichao Wang, Wendong Mao, and Zhongfeng Wang
Shenzhen Campus of Sun Yat-sen University, China

AI1-5 (259) **Layer Sensitivity Mixed-Precision Quantization for Image Super-Resolution**

14:30-14:45

Jun Young Kim, Joo Hyeon Jeon, and Sung In Cho
Dongguk University, Korea

KETI Session

DI2 Crypto & Fault-Tolerant Systems

Chair: Byeong Yong Kong (Kongju National University, Korea)

15:00~16:15, MONDAY_ OCTOBER 13, 2025

NAPOLI (2F)

DI2-1 (9) **VitalSystem: A Fault-Tolerant System Architecture for Wafer-Scale Integration**

15:00-15:15

Yiyang Liu, Jinghe Wei, Wenxin Xu, Leran Wang, Huixiang Li, and Ying Gao
China Electronics Technology Group Corporation, China

DI2-2 (49) **An Area-Time Efficient and Generic Accelerator for the Verification of Hash-Based Signature Schemes**

15:15-15:30

Yueqin Dai[1], Yifeng Song[1], and Zhongfeng Wang[1,2]
[1]*Nanjing University, China*
[2]*Shenzhen Campus of Sun Yat-Sen University, China*

DI2-3 (195) **Scalable and High-Performance Number-Theoretic Transform Design for Lattice-Based Cryptography**

15:30-15:45

Hien Nguyen[1], Quang Dang Truong[2], Hanho Lee[2], and Tuy Tan Nguyen[3,4]
[1]*Northern Arizona University, USA*
[2]*Inha University, Korea*
[3]*Florida A&M University – Florida State University College of Engineering, USA*
[4]*Florida State University, USA*

DI2-4 (239)
15:45-16:00

Design of Robust Clock-Tree Circuit with Transient-Recovery Technique

Junhwa Jeong[1], Jongho Lee[1], Hoyeon Shin[1], Ilho Myeong[2], and Ickhyun Song[1]
[1]*Hanyang University, Korea*
[2]*Myongji University, Korea*

DI2-5 (282)
16:00-16:15

Fast and Energy-Efficient Pipelined Vedic Multiplier Design for Modern Cryptographic Processors

Akkapolu Sankararao, Naveen Kollepara, Vashist Managari, and Binsu J Kailath
IIITDM Kancheepuram, India

OPENEDGES Technology Session

AM2 SAR ADCs and its Building Blocks

Chair: Wonyoung Lee (Seoul National University of Science and Technology, Korea)

15:00~16:15, MONDAY_ OCTOBER 13, 2025

VENICE (2F)

AM2-1 (8)
15:00-15:15

A 66.7dB-SNDR Piplined-SAR ADC with On-Chip Bit-Weight Calibration Achieving ΔSNDR<2.4 Db Across PVT Variations

Jinwei Zhang, Haolin Han, Ruili Ren, Shubin Liu, and Zhangming Zhu
Xidian University, China

AM2-2 (32)
15:15-15:30

A 10-bit 40-MS/s Capacitor-Swapping SAR ADC in 180-nm CMOS

Ying-Liang Li, and Yung-Hui Chung
National Taiwan University of Science and Technology, Taiwan

AM2-3 (154)
15:30-15:45

A 99.1 dB-SNDR CT-DT NS SAR ADC with Two-Stage Stacking Inverter-Cascoded FIA

Yanzhujun Du, Lingxin Meng, Menglian Zhao, and Zhichao Tan
Zhejiang University, China

AM2-4 (193)
15:45-16:00

A 72.7-uW Noise Shaping SAR-Assisted Incremental ADC with Extended Counting Achieving 88.5-dB SNDR and 179.9-dB FoMSNDR

Yi Huo, Menglian Zhao, and Zhichao Tan
Zhejiang University, China

AM2-5 (291)
16:00-16:15

An SSF-Based Fast-Transient LDO as Reference Buffer for a 12-bit 50-MS/s SAR ADC in 40-nm CMOS

Peijuan Ju[1,2], Dixian Zhao[1,2], and Qisong Wu[1,2]
[1]*Southeast University, China*
[2]*Purple Mountain Laboratories, China*

TechwidU Session

AI2 AI/ML Accelerators

Chair: Youngjoo Lee (Korea Advanced Institute of Science and Technology, Korea)

15:00~16:15, MONDAY_ OCTOBER 13, 2025

MIAMI (2F)

AI2-1 (19)
15:00-15:15

An Efficient Accelerator for Attention Mechanism Based on Combined-Head Low-Rank Projection and Unified-PE Candidate Selection

Xingyuan Hu[1], Xulong Zhang[1], Xiao Cong[1], Haoran Geng[1], Chongkang Tan[2], Yuan Du[1], and Li Du[1]
[1]*Nanjing University, China*
[2]*Ant Group, China*

AI2-2 (44)
15:15-15:30

An Energy-Efficient Super-Resolution Processor with Enhanced Tiling Artifact Reduction

Byeungseok Yoo, Sungjin Park, Sunwoo Lee, and Dongsuk Jeon
Seoul National University, Korea

AI2-3 (91)
15:30-15:45

A Dual-Mode High Efficient Hardware Architecture Design for Diffusion Models

Tsung-Lin Tsai, Yi-Cheng Lo, Ching-Yao Chen, and An-Yeu (Andy) Wu
National Taiwan University, Taiwan

AI2-4 (171)
15:45-16:00

ECHO: An Efficient Co-Designed ASR Accelerator with Hardware-Friendly and Audio-Aware Attention

Tseng-Jen Li, and Tian-Sheuan Chang
National Yang Ming Chiao Tung University, Taiwan

AI2-5 (292)
16:00-16:15

Leveraging Natural Structured Sparsity for Energy-Efficient Spiking Transformer Processing

Hyunseok Jung, Dongwoo Lew, and Jongsun Park
Korea University, Korea

LG Electronics Session

AM3 Delta-Sigma ADCs and Power Conversion Techniques

Chair: Jun-Rim Choi (Kyungpook National University, Korea)

16:30 ~ 17:45, MONDAY_OCTOBER 13, 2025

VENICE (2F)

AM3-1 (33)
16:30-16:45

An 88.6-dB SNDR Discrete-Time Delta-Sigma Modulator Using Two-Stage Floating Inverter Amplifiers in 180-nm CMOS

Chun-Yang Chiu, and Yung-Hui Chung
National Taiwan University of Science and Technology, Taiwan

AM3-2 (46)
16:45-17:00

A 17.0-ENOB 400Hz-BW MASH 2-1 ADC with a Time-Multiplexed Nested SDM Quantizer

Zhengzhe Jia, Xinyu Xie, and Zeyu Cai
Peking University, China

AM3-3 (113)
17:00-17:15

Active Time-Constant Error Compensation in Multi-Bit Continuous-Time Delta-Sigma Modulators

Tobias Wolfer, and Eckhard Hennig
Reutlingen University, Germany

AM3-4 (244) **MPPT Boost Converter with AFE for MIC-Based Solar Power Systems**

17:15-17:30

Haechan Park, Jooyun Oh, Jaehyeok Lee, Sungwan Hong, and Joongho Choi
University of Seoul, Korea

AM3-5 (246) **Emulated Peak Current Mode Buck Converter for High Step-Down Applications**

17:30-17:45

Minkwang Ji, Jiho Jung, Jihun Oh, and Joongho Choi
University of Seoul, Korea

Samsung Electronics Session

AI3 AI/ML Algorithms

Chair: Sungju Ryu (Sogang University, Korea)

16:30 ~ 17:45, MONDAY_OCTOBER 13, 2025

MIAMI (2F)

AI3-1 (48) **PROGRESSIVE FEW-SHOT NAS VIA MULTIPLE ELASTIC SUBSUPERNETS FOR EFFICIENT NETWORK SEARCH**

16:30-16:45

Oscal Tzyh-Chiang Chen[1,2], Ya-Yun Cheng[1], Zih-Rong Lin[1], and Manh-Hung Ha[2]
[1]*National Chung Cheng University, Taiwan*
[2]*Vietnam National University, Vietnam*

AI3-2 (109) **Efficient Down-sampling in Hybrid Neural Networks using Adversarial Autoencoders**

16:45-17:00

Jonghyeon Nam[1], Daeheon Lee[1], Joonseok Kim[1], Eunji Kwon[2], and Seokhyeong Kang[1]
[1]*Pohang University of Science and Technology, Korea*
[2]*Kookmin University, Korea*

AI3-3 (220) **Hardware-Aware Backpropagation Training for SNNs on Analog, Ultra-Low Power Neuromorphic Hardware Compensating for Mismatch**

17:00-17:15

Matthias Ochs, Alexander Greif, Max Jamula, and Ralf Brederlow
Technical University of Munich, Germany

AI3-4 (262)
17:15-17:30

APSDCP-Net: Adaptive Patch-Size Dark Channel Prior Network for Single Image Dehazing

Ming-Yang Tu, Kuan-Lin Chen, and Jian-Jiun Ding
National Taiwan University, Taiwan

AI3-5 (331)
17:30-17:45

A Convolutional Autoencoder-based System for Point Cloud Compression

Lih-Jen Kau, and Yong-Wei Liu
National Taipei University of Technology, Taiwan

ETRI Session

RF1 High Performance RF/mm-Wave Oscillators

Chair: Donggu Im (Jeonbuk National Univeristy, Korea)

16:30 ~ 17:45, MONDAY_OCTOBER 13, 2025
CAPRI (2F)

RF1-1 (41)
16:30-16:45

A Dual-Core Mode-Switched L-C Coupled Class-FVCO with 43 % Tuning Range

Kastur Roy[1], Anik Batabyal[2], and Rajesh Zele[1]
[1]*Indian Institute of Technology Bombay, India*
[2]*Silicon Labs, India*

RF1-2 (104)
16:45-17:00

Phase Manipulation VCO Employing Current Harmonic Cancellation Achieving 5 dB Phase Noise Reduction at 1/f^3 Region

Aulya Sholehah Wataawa Sau[1], Hapsah Aulia Azzahra[2], Muhammad Fakhri Mauludin[1], Xi Zhu[3], Jae-won Nam[4], and Jusung Kim[5]
[1]*Hanbat National University, Korea*
[2]*Karlsruhe Institute of Technology, Germany*
[3]*University of Technology Sydney, Australia*
[4]*Seoul National University of Science and Technology, Korea*
[5]*Ewha Womans University, Korea*

RF1-3 (177)
17:00-17:15

Design of a Low Phase Noise Quadrature DCO Using Dual Superharmonic Injection in 55nm CMOS for Ka-Band Applications

Devesh Bhaskaran, and Shashidhar Tantry
PES University, India

RF1-4 (252)
17:15-17:30

A 151.9-165.9 GHz 8.8% FTR Quadrature Voltage Controlled Oscillator in 28-nm FDSOI

Waseem Abbas, Samir Aziri, Christoph Wagner, and Golsa Ghiaasi
Silicon Austria Labs, Austria

RF1-5 (297)
17:30-17:45

A 27 GHz Phase-Coupled Distributed Quad-Core Oscillator in 12 nm FinFET

Valentina Marazzi[1], Lorenzo Porcheddu[1], Marco Garampazzi[2], Enrico Temporiti[2], and Danilo Manstretta[1]
[1]*University of Pavia, Italy*
[2]Marvell Technology Inc, Italy

Regular Sessions (TUESDAY, OCTOBER 14)

Dnotitia Session

DI3 Digital Signal Processing Accelerators

Chair: Hoyoung Yoo (Chungnam National University, Korea)

9:00~10:30, TUESDAY_ OCTOBER 14, 2025

NAPOLI(2F)

DI3-1 (149)
9:00-9:15

A 40nm CMOS PAM-2/4/8 DSP-based Transmitter with 14-tap Feedforward Equalization

Seung-Mo Jin, Dong-Ho Kim, Seung-Hwan Gong, Jae-Geon Lee, Dong-Hyun Lee, Jae-Hyeon Pyeon, In-Ho Han, and Min-Seong Choo
Hanyang University, Korea

DI3-2 (164)
9:15-9:30

pre-Decision Feedforward Equalizer for High-Speed DSP-based Wireline Receiver using Hardware-in-the-Loop Verification on RF-SoC

Jae-Geon Lee, Seung-Hwan Gong, Seung-Mo Jin, Dong-Ho Kim, Dong-Hyun Lee, Jae-Hyeon Pyeon, In-Ho Han, and Min-Seong Choo
Hanyang University, Korea

DI3-3 (199)
9:30-9:45

A Pipeline-Driven FPGA Accelerator with Memory-Scheduling for Neuromorphic Computing

Zhipeng Liao[1], Tianyang Li[2], Ziyang Shen[1,3], Chaoming Fang [1,3], Jie Yang [1,2,3], and Mohamad Sawan[1,2,3]
[1]Westlake University, China
[2]Westlake Institute for Optoelectronics, China
[3]Integrated-On-Chips Brain-Computer Interfaces Zhejiang Engineering Research Center, China

DI3-4 (216)
9:45-10:00

Binary-Encoding Based Scalable Digital Ising Machine for Traveling Salesman Problems: Spin-Efficient and Fast Convergence

Wentao Huang, Kaili Zhang, Lang Zeng, Bolin Zhang, Yu Liu, Bojun Zhang, Jinkai Wang, Yue Zhang, Youguang Zhang, Weisheng Zhao, and Deming Zhang
Beihang University, China

DI3-5 (218)
10:00-10:15

A Quantitative Evaluation Method of Neural Rendering Accelerators

Hayun Oh[1], and Youngjoo Lee[2]
[1]*Pohang University of Science and Technology, Korea*
[2]*Korea Advanced Institute of Science and Technology, Korea*

DI3-6 (349)
10:15-10:30

CoRN-LN: Compressed Reciprocal Newton Method for Efficient Layer Normalization

Dawon Choi, Hana Kim, and Ji-Hoon Kim
Hanyang University, Korea

ETRI Session

PE Power and Energy Circuits and Systems

Chair: Seungkyu Choi (Kyung Hee University, Korea)

9:00~10:30, TUESDAY_ OCTOBER 14, 2025

VENICE (2F)

PE-1 (95)
9:00-9:15

A High PSR LDO with Adaptive Feedforward Ripple Cancellation and Error Amplifier Noise Cancellation

Hung-Ju Lee, Liang-Kai Wang, and Kea-Tiong Tang
National Tsing Hua University, Taiwan

PE-2 (105)
9:15-9:30

A Hybrid Buck-Boost Converter with Single Duty Cycle Control and Continuous Output Current

Tiantian Tang[1], Chen Hu[1], Ming Yu[1], Xun Liu[2], and Junmin Jiang[1]
[1]*Southern University of Science and Technology, China*
[2]*The Chinese University of Hong Kong, China*

PE-3 (165)
9:30-9:45

A Three-Level Inverting Buck Converter with 5μs Response Time and 20mV Output Ripple for Micro-LED Displays

Gang Liu[1], Wuxiao Dong[1], Ruidong Li[2], Guoqing Li[2], Junmin Jiang[3], and Xun Liu[1]
[1]*The Chinese University of Hong Kong, China*
[2]*Shandong Yunhai Guochuang Cloud Computing Equipment Industry Innovation Company Ltd., China*
[3]*Southern University of Science and Technology, China*

PE-4 (201)
9:45-10:00

A 5V-to-1V Hybrid Buck Converter with Asynchronized Switched Inductors and Hybrid Controls for Fast Load Transient

Haoqiang Deng[1], Ming Yu[1], Ruidong Li[2], Chen Hu[1], Guoqing Li[2], Xun Liu[3], and Junmin Jiang[1]
[1]*Southern University of Science and Technology, China*
[2]*Shandong Yunhai Guochuang Innovative Technology Co., Ltd., China*
[3]*The Chinese University of Hong Kong, China*

PE-5 (251)
10:00-10:15

A Discontinuously Resonant Operation for Continuously-Scalable-Conversion-Ratio Switched Capacitor Converter with Enhanced Power Efficiency and Output Capability

Haozhe Zhang[1], Chuang Wang[2], Xiaosen Liu[1], Xuliang Wang[1], Renwei Chen[1], Xuchen Men[1], Feng Wang[2], and Yan Wang[1]
[1]*Tsinghua University, China*
[2]*Huawei Technologies Co., Ltd, China*

PE-6 (266)
10:15-10:30

Advanced Voltage Measurement Unit with On-Chip High-Pass Filters for Battery EIS System

Byeongho Hwang, Yunchae Lee, Jihan Shin, Jinho Park, Uikyoung Lee, and Kyeongha Kwon
Korea Advanced Institute of Science and Technology, Korea

ASICLAND Session

AI4 PIM/CIM Systems

Chair: Seokhyeong Kang (Pohang University of Science and Technology, Korea)

9:00~10:30, TUESDAY_ OCTOBER 14, 2025

MIAMI (2F)

AI4-1(22)
9:00-9:15

Energy-Efficient ReRAM-based In-Memory Computing with Dual SNN/ANN Modes

Chang-Yu Kuo, Tian-Sheuan Chang, and Tsung-Heng Tsai
National Yang Ming Chiao Tung University, Taiwan

AI4-2 (65)
9:15-9:30

A 6T SRAM Analog CIM Macro for 8-bit MAC with Input/Weight Partitioning for High Signal Margin and Throughput

Abhishek Goel, Cheena Singhal, Dinesh Kushwaha, Sparsh Mittal, and Sudeb Dasgupta
Indian Institute of Technology Roorkee, India

AI4-3 (190)
9:30-9:45

ETA: Efficient Transformer Attention Mapping for ReRAM-based Compute-In-Memory Architectures

Johnny Rhe, Juhong Park, Kang Eun Jeon, and Jong Hwan Ko
Sungkyunkwan University, Korea

AI4-4 (217)
9:45-10:00

IR-aware Weight Remapping Considering Thermal Effect and Stuck-at Faults in RRAM Crossbar Array

Shih-Han Chang, Yi-Lun He, and Chien-Nan Jimmy Liu
National Yang Ming Chiao Tung University, Taiwan

AI4-5 (222)
10:00-10:15

A 28nm 20 TOPS/W In-Memory Search Engine with Pre-Charge-Free SRAM-based TCAM and Hybrid-Match Mechanism for Few-Shot Learning

Jen-Chieh Wang[1], Chi-Tse Huang[1], Chia-Wei Su[2], Chun-Fu Chen[3], I-Chyn Wey[2], Hsiang-Yun Cheng[4], and An-Yeu (Andy) Wu[1]
[1] *National Taiwan University, Taiwan* [2] *Chang Gung University, Taiwan*
[3] *National Taiwan University of Science and Technology, Taiwan*
[4] *Academia Sinica, Taiwan*

AI4-6 (293) 10:15-10:30

Bit-Preserving Analog Alignment-Based Cross-Domain FP-CIM for LLMs

Huiwon Kim, Dongwoo Lew, and Jongsun Park
Korea University, Korea

Samsung Electronics Session

AM4 Analog Amplifiers and Filters

Chair: Jusung Kim (Ewha Womans Univ., Korea)

13:30~14:45, TUESDAY_ OCTOBER 14, 2025

GRAND BALL ROOM (2F)

AM4-1 (18) 13:30-13:45

A Sub-Threshold Tunable Band-Pass Filter for Low- Power Audio Signal Processing

Ahmed Reda Mohamed
KFUPM, Saudi Arabia

AM4-2 (174) 13:45-14:00

A 55 MHz-Bandwidth Sub-μV-Offset High-Precision Amplifier with Two-step Automatic Offset Calibration

Yang Zhang, Zi Wang, and Mingyi Chen
Shanghai Jiao Tong University, China

AM4-3 (183) 14:00-14:15

A Temperature-Stabilized Gm Technique for Folded-Cascode OTAs in 22nm FDSOI Technology

Claire Mahusay, Cedric Allen Oria, Arcel Leynes, Maria Sophia Ralota, Vincent Angelo Bogg's Roxas, Marc Rosales, and Maria Theresa de Leon
University of the Philippines Diliman, Philippines

AM4-4 (267) 14:15-14:30

A 12-μV Offset Low-Input-Bias-Current High-Precision CMOS Operational Amplifier with Automatic Offset Calibration

Kunxun Luo, Jingquan Liu, and Jingquan Liu
Shanghai Jiao Tong University, China

AM4-5 (296)
14:30-14:45

A Low Power, Bandwidth Enhanced, Negative-R Assisted Fourth Order Active-RC Filter

Sayyad Arif[1,5], Nagaveni S[2], Soumya Gupta[3,5], and Manjunath Kareppagoudr[4,5]
[1]*Sahyadri College of Engineering and Management, India*
[2]*Indian Institute of Technology, India*
[3]*Oregon State University, USA*
[4]*Sensesemi Technologies, India*
[5]*CuriousIC Edu, India*

DeepX Session

RF2 RF Transceivers and Building Blocks

Chair: Jaeho Im (Hongik University, Korea)

13:30~14:30, TUESDAY_ OCTOBER 14, 2025

NAPOLI (2F)

RF2-1 (83)
13:30-13:45

A 63.6-81 GHz Broadband LNA with 22.9 dB Gain and 4.9 dB NF in a 65-nm CMOS Technology

Guanglai Wu[1,2], Yun Fang[2,3], Zongming Duan[4], Yi Zhang[1], Yufeng Guo[1], Yongjie Li[2], and Hao Gao[1,2,3,5]
[1]*Nanjing University, China*
[2]*Purple Mountain Laboratory, China*
[3]*Southeast University, China*
[4]*East China Research Institute of Electronic Engineering, China*
[5]*Eindhoven University of Technology, Netherlands*

RF2-2 (125)
13:45-14:00

K-Band 65-nm CMOS 2-Stage LNA Using High- Pass Filter for Low-Noise and Neutralization Capacitor for Wideband Performance

Chaeyun Kim, Hyojin Yoon, Jaeyong Lee, and Changkun Park
Soongsil University, Korea

RF2-3 (241)
14:00-14:15

A V-Band Noise Canceling LNA for Atmospheric Temperature Profiling Radiometers

Mounika Kare[1], Anik Batabyal[2], and Rajesh Zele[1]
[1]*Indian Institute of Technology Bombay, India*
[2]*Silicon Labs Hyderabad, India*

RF2-4 (273)
14:15-14:30

A 2-4GHz Wideband Transmitter Front-End for FMCW Through-wall Radar Applications

Yunqi Yang[1], Haoyu Shen[2], Hao Lei[1], Zhigang Fu[1], Pengcheng Wang[1], Yilin Xu[1], Fanxun Cai1, Xiao Fang[1], and Hui Zhang[1]
[1]*Beihang University, China*
[2]*Instite of Microelectronics of the Chinese Academy of Sciences, China*

TechwidU Session

AM5 High-speed Wireline Techniques

Chair: Junghyup Lee (Daegu Gyeongbuk Institute of Science & Technology, Korea)

13:30~14:45, TUESDAY_ OCTOBER 14, 2025

VENICE (2F)

AM5-1 (129)
13:30-13:45

A Booster-Enhanced Mismatch-Canceling Latch-Based True Random Number Generator for High-Speed Operation

Yutao Deng, and Mahfuzul Islam
Institute of Science Tokyo, Japan

AM5-2 (148)
13:45-14:00

A 20-to-32-Gb/s 1.37 pJ/bit PI-based CDR with a Direct Proportional Path and an IIR Filter for Low Latency and Wide ppm Tracking in 28-nm CMOS

Seung-Hwan Gong, Dong-Hyun Lee, Seung-Mo Jin, Dong-Ho Kim, Jae-Geon Lee, In-Ho Han, Jae-Hyeon Pyeon, and Min Seong Choo
Hanyang University, Korea

AM5-3 (159)
14:00-14:15

A 112Gb/s PAM4 Mach-Zehnder modulator Driver in 12nm FinFET with 3.8V Output Swing for Analog-Digital Co-integration

Giovanni Marco Rubino, Alessio De Pr`a, and Danilo Manstretta
University of Pavia, Italy

AM5-4 (236)
14:15-14:30

A 56 Gb/s PAM-4 CDR Circuit using Middle Transition Masking and Integrated Bit Decoding Schemes

Seung-Gyun Kim, and Won-Young Lee
Seoul National University of Science and Technology, Korea

OPENEDGES Technology Session

BM Biomedical Circuits and Systems

Chair: Seong-Jin Kim (Sogang University, Korea)

13:30~14:45, TUESDAY_ OCTOBER 14, 2025
MIAMI (2F)

BM-1 (118)
13:30-13:45

A Reconfigurable 8-Channel Dual-Mode Neural Stimulator with High-Voltage Compliance and 97% Efficiency

Yijun Ye[1], Yutao Mao[1], Wenjun Zou[2], Hui Wu[2], Xing Liu[2], Ziqi Tan[1], Mostafa Katebi[4], Jie Yang[2,3], and Mohamad Sawan[1,2,3]
[1]*Westlake Institute for Optoelectronics, China*
[2]*Westlake University, China*
[3]*Integrated-on-Chips Brain-Computer Interfaces Zhejiang Engineering Research Center, China*
[4]*Iran University of Science and Technology, Iran*

BM -2 (138)
13:45-14:00

A Non-Invasive Ultrasound-Transmission-Based Thermometry Method for Multi-Layer Deep Tissue Monitoring

Saebyeok Shin, Jaehong Jung, Mohith Manohara, Anantha P. Chandrakasan, and Ahmad Bahai
University of Cambridge, USA

BM -3 (167)
14:00-14:15

A Continuous-Wave/Frequency-Domain Reconfigurable Light-Sensing Readout Circuit for Functional Biomedical Imaging Application

Wenzhe Qin, Huanyu You, Sibo Peng, Xiafan Gu, Eva Guttmann-Flury, Jiajun Yuan, and Jian Zhao
Shanghai Jiao Tong University, China

BM -4 (188)
14:15-14:30

Low Fractional Spurs Frequency Synthesizer for Nuclear Magnetic Resonance Measurement Systems

Parham Davami, Guillaume Mocquard, and Thomas Burger
Federal Institute of Technology Zurich, Switzerland

BM -5 (276)
14:30-14:45

A 16-Channel TDM Spectral Feature Extraction Using IIR Filter for Closed-loop Neuromodulation

Tarun Choudhary, Lakshmi Iyer, and Laxmeesha Somappa
Indian Institute of Technology Bombay, India

Furiosa AI Session

CM Beyond CMOS: Nanoelectronics and Hybrid Systems Integration

Chair: Mahfuzul Islam (Institute of Science Tokyo, Japan)

15:00~16:15, TUESDAY_ OCTOBER 14, 2025

NAPOLI (2F)

CM-1 (55)
15:00-15:15

A High-Performance RRAM-Based PMM Accelerator for Lattice-Based PQC

Yang Chen, Zeren Zhu, Bei Wang, Chenghua Wang, and Yijun Cui
Nanjing University of Aeronautics and Astronautics, China

CM-2 (62)
15:15-15:30

A DL-MRBL Scheme with Variation-Resilient Timing for Wide Voltage STT-MRAM

Ruiqi Zhang, Shuyu Wang, Haoran Du, and Hao Cai
Southeast University, China

CM-3 (85)
15:30-15:45

Multi-Channel Quantum-Effect Thin-Film Transistors for beyond CMOS Applications

Mohammad Masum Billah[1], Moath Alathbah[2], Jung Bae Kim[3], and Jin Jang[4]
[1]*Islamic University, Bangladesh*
[2]*King Saud University, Saudi Arabia*
[3]*Applied Materials Inc., USA*
[4]*Kyung Hee University, Korea*

CM-4 (142)
15:45-16:00

An Enhanced ASAP7 PDK with PowerVia Technology for IR Drop and PPA Evaluation

Mingjie Yu, Jiaqi Dou, Bingyi Ye, Yang Shen, Xiaojin Li, Yanling Shi, Yuhang Zhang, and Yabin Sun
East China Normal University, China

CM-5 (231)
16:00-16:15

Design Automation for a-IGZO Thin Film Technology using a Multi-row Standard Cell Architecture

Yi-Ting Lin[1], Yalun Tang[2], Byeonggon Kang[3], Iris Hui-Ru Jiang[1], Kenji Nomura[2], Yuhwa Lo[2], Lifu Chang[4], Bill Lin[2], and Chung-Kuan Cheng[3]
[1]*National Taiwan University, Taiwan*
[2]*University of California San Diego, USA*
[3]*University of California San Diego, USA*
[4]*The MOSIS Service, USA*

LG Electronics Session

AM6 Emerging Computing Systems

Chair: Younghyun Lim (Kyunghee University, Korea)

15:00~16:15, TUESDAY_ OCTOBER 14, 2025

VENICE (2F)

AM6-1 (61)
15:00-15:15

Advanced Techniques for Mitigating Power Supply Induced Jitter in Low-Cost, Multi-Lane, Multi-PHY Timing Controller Solutions in 8 nm FinFET

Subhadeep Datta[1], Ankur Ghosh[1], A Santosh Kumar Reddy[1], Umamaheswara Reddy Katta[1], Manohar Seetharam[1], Byunghyun Lim[2], Jongjae Ryu[2], Goeun kim[2], Doohee Lim[2], Sachin Kashyap[1], Mohit Arora[1], Bhargavi SPH[1], Saikat Hazra[1], Sumanth Chakkirala[1], and Avneesh Singh Verma[1]
[1]*Samsung Semiconductor India Research, India*
[2]*Samsung Electronics, Korea*

AM6-2 (67)
15:15-15:30

ChargeFloat-TQ: A Charge-Domain-Based Tracking-Quantized Floating-Point Computing-in-Memory Accelerator Macro

Yu Liu[1,2], Hao Li[1], Changxin Yue[1], Xiulong Wu[1,2], Chunyu Peng[1,2], Wenjuan Lu[1,2], Chenghu Dai[1,2], Xin Li[1,2], and Zhiting Lin[1,2]
[1]Anhui University, China
[2]The Anhui High-performance Integrated Circuit Engineering Research Center, China

AM6-3 (140)
15:30-15:45

A 10T SRAM-Based PUF Enhanced by In-Memory Computing for Secure Authentication

Neha Maheshwari[1], Shivam Vaish[1], Kwok Tai Chui[2], Brij Bhooshan Gupta[3], and Santosh Kumar Vishvakarma[1]
[1]Indian Institute of Technology Indore, India
[2]Hong Kong Metropolitan University, Hong Kong
[3]Asia University, Taiwan

AM6-4 (156)
15:45-16:00

A Signed-Transfer SRAM Computing-In-Memory Macro with In-Column Reconfiguration DAC and 2bit/Cycle Quantization

Ying Pan, Xin Li, Yuanyang Wang, Jiaqi Chen, Yang Lou, Yifan Wu, Jianxing Zhou, Qiushi Feng, Wenqiang Zhang, Baofa Wu, Chenghu Dai, Yu Liu, Xiulong Wu, and Zhiting Lin
Anhui University, China

AM6-5 (158)
16:00-16:15

A 3T2C eDRAM CIM Macro with Configurable Sensing and Calibration for Ternary Neural Network

Dong-Hyun Lee, Seung-Mo Jin, Dong-Ho Kim, Seung-Hwan Gong, Jae-Geon Lee, In-Ho Han, Jae-Hyeon Pyeon, and Min-Seong Choo
Hanyang University, Korea

Furiosa AI Session

SN Sensory, Neural, and Nonlinear Circuits and Systems

Chair: HIdeaki Okazaki (Shonan Institute of Technology, Japan)

15:00~16:15, TUESDAY_ OCTOBER 14, 2025

MIAMI (2F)

SN-1 (97)
15:00-15:15

3ETSS: An Energy-Efficient Event-based Tactile Sensing System

Yuncheng Lu[1], Kiho Seong[1], Chufeng Yang[1], Junying Li[1], Zechen Wang[1], Si En Timothy Ng[1], Shibi Varku[1], Arindam Basu[2], Nripan Mathews[1], and Tony Tae Hyoung Kim[1]
[1]*Nanyang Technological University, Singapore*
[2]*City University of Hong Kong, Hong Kong*

SN-2 (283)
15:15-15:30

A 65nm 0.0736mm2/Pixel Simultaneous Energy-Harvesting-and-Sensing 2-by-2 Self-Powered CMOS Image Sensor Pixel Array Using Self-Oscillating Voltage Doubler for Thermal-Aware Zero-Stand-by-Power Imaging

Kei Awano[1], Yoshitsune Sugimura[1], Yuma Ota[1], You Wu[1], Keishi Ogura[1], Hiroaki Kitaike[1], Kento Okamura[1], Shufan Xu[1], Jin Nakamura[2], Masaya Kaneko[2], Yuta Kimura[3], Hiroaki Nakamura[3], Ruilin Zhang[1], Hirofumi Shinohara[1], Kunyang Liu[1], and Kiichi Niitsu[1]
[1]*Kyoto University, Japan*
[2]*Meitec Corp., Japan*
[3]*Shuhari System Inc., Japan*

SN-3 (82)

Periodic orbits and Hardware Implementation of Permutation XOR Cellular Automata

Yosuke Suzuki, and Toshimichi Saito
Hosei University, Japan

SN-4 (103)
15:45-16:00

FPGA Implementation and Analysis on Parallel and Pipeline Approximate Softmax for Transformer

Abdullah Celep[1,2], Trio Adiono[1], Infall Syafalni[1], Nana Sutisna[1], Nur Ahmadi[1], and Rahmat Mulyawan[1]
[1]*Bandung Institute of Technology, Indonesia*
[2]*Technical University of Munich, Germany*

SN-5 (237)
16:00-16:15

THES-SNN: Thresholded Hybrid Encoding with Single-Spike Neurons for Energy-Efficient Spiking Neural Networks

Jia Yu, Tianyang Yu, Bi Wu, Ke Chen, Chenggang Yan, and Weiqiang Liu
Nanjing University of Aeronautics and Astronautics, China

ASICLAND Session

DI4 Computation Optimization

Chair: Yeong-kyo Seo (Inha University, Korea)

16:30~17:45, TUESDAY_ OCTOBER 14, 2025

NAPOLI (2F)

DI4-1 (98)
16:30-16:45

BWFA-CAT: Bidirectional Wavefront Sequence Alignment with Content-Aware Tiling and Its Hardware Accelerator

Chia-Hung Lin, Po-Yen Chang, and Yi-Chang Lu
National Taiwan University, Taiwan

DI4-2 (135)
16:45-17:00

Posit adder and multiplier with variable input and output exponent sizes

Min Kee Chang[1], Dae Ryong Shin[1], HyunJin Kim[1], and Alberto A. del Barrio[2]
[1]Dankook Univeristy, Korea
[2]Complutense University of Madrid, Spain

DI4-3 (160)
17:00-17:15

A Hardware-Efficient Approximate LMS-FFE for PAM4 Optical Communication Systems

Yunjie Zhao, Hongfei Sun, Rong Wu, Ke Chen, Bi Wu, and Chenggang Yan
Nanjing University, China

DI4-4 (228)
17:15-17:30

Hardware-Efficient VLSI Architecture for L-BFGS Detection in MIMO-OFDM Systems

Xuenan Wang, Yijing Yang, Chenggang Yan, Bi Wu, and Ke Chen
Nanjing University of Aeronautics and Astronautics, China

DI4-5 (281)
17:30-17:45

A Configurable RISC-V Vector Processor with FSM-Driven Accelerator for Data-Intensive Workloads

Akkapolu Sankararao, Vashist Managari, Naveen Kollepara, and Binsu J Kailath
Indian Institute of Technology Madras, India

AM7 Sensors and Precision References

Chair: Jusung Kim (Ewha Womans University, Korea)

16:30~17:45, TUESDAY_ OCTOBER 14, 2025

VENICE (2F)

AM7-1 (11)
16:30-16:45

A Sub-1-V 2-Bit Low-Noise and High-PSRR Low-Dropout Linear Regulator in 65-nm SOI CMOS for 5G Applications

Li Dai[1,2], Jin Li[1,2,3], Bo Chen[1,2], Linqian Zhao[1,2], and Tao Yuan[1,2,3]
[1]*Shenzhen University, China*
[2]*Guangdong-Hong Kong Joint Laboratory for Big Data Imaging and Communication, China*
[3]*State Key Laboratory of Millimeter Waves, China*

AM7-2 (71)
16:45-17:00

A 0.01 mm2 RC-Filter-Based Temperature Sensor with Phase-Domain DSM Readout Achieving 232fJ·K2 Resolution FoM

Shuan Yang[1], Tai-Hong Chen[1], Yu-Chi Wang[1], Chia-Hsi Fang[1], Chun-Yu Lin[1], Shan-Chih Tsou[2], Shon-Hang Wen[2], Kuan-Dar Chen[2], and Tsung-Hsien Lin[1]
[1]*National Taiwan University, Taiwan*
[2]*MediaTek, Taiwan*

AM7-3 (93)
17:00-17:15

A 1.86ppm/℃ CMOS-Only Voltage Reference with 20mA Load Driving Capability

Huiqi Chen[1], Zhaonan Lu[1], Zili Zhou[1], Jiankao Pan[2], Shuang Song[1], and Menglian Zhao[1]
[1]*Zhejiang University, China*
[2]*Zhejiang Transsemi Microelectronics Co., Ltd, China*

AM7-4 (189)
17:15-17:30

A CMOS SOI 180nm Sub-ranging Bandgap Reference with 4.5ppm/°C TC across −40 to 175°C

Mingrui Wang[1], Hengchen Zou[1], Rui Martins[1,2], Pui-In Mak[1], and Ka-Meng Lei[1]
[1]*University of Macau, China*
[2]*Universidade de Lisboa, Portugal*

AM7-5 (258)
17:30-17:45

A 3.35 and 4.18 ppm/oC Dual-output Bandgap Reference Circuit with Wide Temperature Range Using Curvature and Digital PVT Compensation

Tzung-Je Lee[1], Zi-Yi Huang[1], Aleksandr Vasjanov[2], and Vaidotas Barzdenas[2]
[1]*National Sun Yat-Sen University, Taiwan*
[2]*Vilnius Gediminas Technical University, Lithuania*

AI5 Emerging AI/ML Solutions

Chair: Injae Yoo (Busan National University, Korea)

16:30~17:45, TUESDAY_ OCTOBER 14, 2025

MIAMI (2F)

AI5-1 (106)
16:30-16:45

A 1D Lightweight ShuffleNetV2 for Cardiovascular Disease Detection in a Point-of-Care System

Feng Jiang[1], Yang Wei Lim[1], Siti Anom Ahmad[1], Faisul Arif Ahmad[1], Luthffi Idzhar Ismail[1], Ahmed Faeq Hussein[2], and Fakhrul Zaman Rokhani[1]
[1]*University Putra Malaysia, Malaysia*
[2]*Al-Nahrain University, Iraq*

AI5-2 (150)
16:45-17:00

CLCO-S1: Efficient Softmax1 Architecture of Cross Level Collaborative optimization for Transformer

Yingqian Chen[1], Haoran Geng[2], Cheng Liu[1], and Li Du[2]
[1]*Shanghai University, China*
[2]*Nanjing University, China*

AI5-3 (221)
17:00-17:15

A Memory-Efficient Framework for Deformable Transformer with Neural Architecture Search

Wendong Mao[1], Mingfan Zhaoa[1], Jianfeng Guan[1], Qiwei Dong[2], and Zhongfeng Wang[1]
[1]*Shenzhen Campus of Sun Yat-Sen University, China*
[2]*Nanjing University, China*

AI5-4 (253)
17:15-17:30

Uncertainty-Aware Performance Evaluation of Low-Noise Amplers via Generalized Polynomial Chaos Expansion-based Surrogate Model

Hoyeon Shin[1], Taeyeong Kim[1], Jiyong Chung[1], Moon-kyu Cho[2], Songnam Hong[1], and Ickhyung Song[1]
[1]*Hanyang University, Korea*
[2]*Korea National University of Transportation, Korea*

AI5-5 (338)
17:30-17:45

Memory-Efficient Differential Privacy Accelerator

Muhammad Hamis Haider[1], Nam-joon kim[2], Hao Zhang[3], Janier Arias-Garcia[4], Hyuk-Jae Lee[2], and Seok-Bum Ko[1]
[1]*University of Saskatoon, Canada*
[2]*Seoul National University, Korea*
[3]*Ocean University, China*
[4]*Universidade Federal de Minas Gerais, Brazil*

Special Sessions (MONDAY, OCTOBER 13)

SS1 Advanced RF Transceiver Circuits for Next-Generation Wireless Systems

Organizer: Heein Yoon (Ulsan National Institute of Science and Technology, Korea)

Chair: Heein Yoon (Ulsan National Institute of Science and Technology, Korea)

13:30~14:45, MONDAY_OCTOBER 13, 2025

CAPRI (2F)

SS1-1 (69) 13:30-13:45

A 5.74–8.02 GHz Area-Efficient and Low-Noise CMOS Cross-Coupled LC-VCO

Hyogyoung An, Hyeonjun Nam, Sungjin Kim, and Heein Yoon
Ulsan National Institute of Science and Technology, Korea

SS1-2 (108) 13:45-14:00

A Sub-Sampling Fast Lock Detector for Fractional-N PLL

Fanxun Cai, Ziyang Li, Zijie Wang, Yunqi Yang, Pengcheng Wang, Yilin Xu, Lianbo Wu, and Hui Zhang
Beihang University, China

SS1-3 (141) 14:00-14:15

A Ka-band Low-Noise Amplifier with Co-optimized Magnetic-Coupled Gm-Boosting and Parallel Inductor for 5G FR2 and 6G LEO SATCOM

Kyoungwoo Kim, Jungro Lee, Jinseok Park, and Seungchan Lee
Chonnam National University, Korea

SS1-4 (161) 14:15-14:30

IR-UWB Transceivers for Energy-Efficient Wireless Communication

Minyoung Song
Daegu Gyeongbuk Institute of Science & Technology, Korea

SS1-5 (169) 14:30-14:45

Hybrid LDO having Small-Output Ripple and Fast-Settling at 0.5V Supply Using Dynamic Gate-Voltage Generation and Fast-PD Decision

Seungwan Kim, and Younghyun Lim
Kyung Hee University, Korea

SS2 Circuits and Applications for Energy-Efficient Edge Systems

Organizers: Chung-An Shen (National Taiwan University of Science and Technology, Taiwan)

Chair: Chung-An Shen (National Taiwan University of Science and Technology, Taiwan)
Shanq-Jang Ruan (National Taiwan University of Science and Technology, Taiwan)

13:30~14:45, MONDAY_OCTOBER 13, 2025

SICILY (1F)

SS2-1 (17)
13:30-13:45

Implementation and Analysis of Mandarin Lipreading on Edge Devices

Yu-Hsuan Tseng, Che-Min Tsai, Chong-Hao Xu, and Shang-Jang Ruan
National Taiwan University of Science and Technology, Taiwan

SS2-2 (42)
13:45-14:00

A Highly Efficient LMS Equalizer for IEEE 802.15.4a/z UWB Wireless Communication Systems

Yen-Hsun Tsai, Wenn-Yi Lin, and Chung-An Shen
National Taiwan University of Science and Technology, Taiwan

SS2-3 (121)
14:00-14:15

Accuracy-Enhanced Block Spiking Neural Networks with Convolutional Localized Inhibition

Chia-Hsuan Mi[1], Tsu-Ping Lin[2], Tsu-Chiao Chen[1], and Kun-Chih (Jimmy) Chen[1]
[1]*National Yang Ming Chiao Tung University, Taiwan*
[2]*National Sun Yat-sen University, Taiwan*

SS2-4 (137)
14:15-14:30

Codeword-Aware Data Mapping for Efficient JPEG Decoding on Skyrmion Racetrack Memory

Wan-Siang Wu, Yu-Ting Huang, Yu-Rou Shen, and Yu-Pei Liang
National Chung Cheng University, Taiwan

SS2-5 (245)
14:30-14:45

Design Navigation and Exploration of Complementary Ferroelectric FET (CFeFET) for Next-Generation CFET-based Nonvolatile SRAM and Logic-in Memory Applications

Yung-Hsuan Huang, Chu-Hsiu Hsu, Yuan-Yu Huang, Pin Su, and Po-Tsang Huang
National Yang Ming Chiao Tung University, Taiwan

SS3 Display Driver and Touch Readout Circuits

Organizers: Hyun-Sik Kim (Korea Advanced Institute of Science and Technology, Korea)

Chair: Hyun-Sik Kim (Korea Advanced Institute of Science and Technology, Korea)

15:00~16:15, MONDAY_ OCTOBER 13, 2025

CAPRI (2F)

SS3-1 (64)
15:00-15:15

A 10b Source-Driver IC with All-Channel Automatic Offset Calibration and Slew-Rate-Enhanced Amplifier for 6285-PPI OLED-on-Silicon Displays

Junghwan Oh, Dong-Kun Lee, and Jong-Seok Kim
Hanyang University ERICA, South Korea

SS3-2 (68)
15:15-15:30

A Display Source-Driver IC Featuring Multistage-Cascaded 10-Bit DAC and True-DC-Interpolative Super-OTA Buffer

Seunghwa Shin, and Hyun-Sik Kim
Korea Advanced Institute of Science and Technology, Korea

SS3-3 (76)
15:30-15:45

An Area and Power Efficient 10-bit Column Driver IC for Mobile AMOLED Displays

Seung Hun Choi, Jaewoong Ahn, Seo Young Lee, and Hyung-Min Lee
Korea University, Korea

SS3-4 (110)
15:45-16:00

Design of Touch-Sensor Interface ICs for Next-Generation Displays

Taeho Lee, and Jun-Eun Park
Sungkyunkwan University, Korea

SS3-5 (155)
16:00-16:15

A Perspective on Self-Capacitive Readout Architectures for In-Cell Touch Panels

Jun Seong Kim, Dabin Yun, Sang Weun Kim, Wooseok Jang, Hamin Lee, and Seunghoon Ko
Kwangwoon University, Korea

SS4 Software-Hardware Co-Design for Neural Networks

Organizers: Sungju Ryu (Sogang University, Korea)

Chair: Sungju Ryu (Sogang University, Korea)

15:00~16:15, MONDAY_ OCTOBER 13, 2025

SICILY (1F)

SS4-1 (15)
15:00-15:15

Exploiting Timestep Similarity for Efficient Diffusion Transformer Acceleration

Youngjun Park, Sangyeon Kim, Yeonggeon Kim, Gisan Ji, and Sungju Ryu
Sogang University

SS4-2 (16)
15:15-15:30

Leveraging Gustavson's Algorithm for Efficient SNN Acceleration with Column-Parallel Tick-Batch

Donghun Lee, Sangwoo Hwang, and Jaeha Kung
Korea University, Korea

SS4-3 (28)
15:30-15:45

A Reinforcement Learning Processor for Mobile Robots

Juyoung Oh, and Dongsuk Jeon
Seoul National University, Korea

SS4-4 (133)
15:45-16:00

Memory-Aware Vector Mapping for Efficient Matrix Multiplication on RISC-V Vector Extension

Gyuhyun Jung[1], Jaehee Kim[1], Youngjoo Lee[2], and Seungsik Moon[3]
[1]*Pohang University of Science and Technology, Korea*
[2]*Korea Advanced Institute of Science and Technology, Korea*
[3]*Chungbuk National University, Korea*

SS4-5 (249)
16:00-16:15

Efficient Token Pruning for Large Vision-Language Models in Multi-turn Scenarios

Changwoo Baek[1], Sohyen Kim[1], Jou Won Song[2], and Kyeongbo Kong[1]
[1]*Pusan National University, Korea*
[2]*LG Electronics, Korea*

SS5 Next-Generation Circuit Techniques: From Analog and Power to Digital Compute

Organizers: Junghyup Lee (Daegu Gyeongbuk Institute of Science and Technology, Korea)

Chair: Junghyup Lee (Daegu Gyeongbuk Institute of Science and Technology, Korea)

16:30~17:45, MONDAY_OCTOBER 13, 2025
SICILY (1F)

SS5-1 (24)
16:30-16:45

A 65nm 687.5-TOPS/W Drive Strength-based SRAM Compute-In-Memory Macro with Adaptive Dynamic Range for Edge AI applications

Dong-Gu Choi[1], Jaehyun Lee[1], Jahyun Koo[1], Dahoon Park[2], Woo-Kyoung Han[2], Jaeha Kung[2], Junghyup Lee[1], and Jong-Hyeok Yoon[1]
[1]Daegu Gyeongbuk Institute of Science and Technology, Korea
[2]Korea University, Korea

SS5-2 (30)
16:45-17:00

An Energy-Efficient Continuous-Time Noise-Shaping SAR Capacitance-to Digital Converter

Gichan Yun[1], Sohmyung Ha[2], and Minkyu Je[1]
[1]Korea Advanced Institute of Science and Technology, Korea
[2]New York University Abu Dhabi, United Arab Emirates

SS5-3 (45)
17:00-17:15

A 90-260 VAC Isolated Offline Single-Stage Single-Transformer-Winding Multiple-Output (STWMO) RGBW LED Driver with <0.7% Current Variation and Dimmable Error-Based Control

Mun-Jung Cho[1], Changsik Shin[2], Seung-Ju Lee[1], Jong-Hun Kim[1], Yeon-Woo Jeong[1], Min-Sik Kim[1], Myeong-Ho Kim[1], Hyuntak Jeon[3], and Se-Un Shin[1]
[1]Pohang University of Science and Technology, Korea
[2]Samsung Electronics, Korea
[3]Chungbuk National University, Korea

SS5-4 (50)
17:15-17:30

A 3.3-to-11V-Supply-Range 10μW/Ch Arbitrary-Waveform-Capable Neural Stimulator with Output-Self-Bias and Supply-Tracking Scheme in 0.18μm Standard CMOS

Jeongyoon Wie, and Junghyup Lee
Daegu Gyeongbuk Institute of Science and Technology

SS5-5 (127)

17:30-17:45

A Hybrid Step-Down DC-DC Converter for High Input-Voltage and High Voltage-Conversion-Ratio Applications

Seunghoon Lee[1], Seungjin Baek[1], Seongil Yeo[1], Woojin Jang[2], Sungbeom Kim[3], and Kunhee Cho[1]

[1]*Sungkyunkwan University, Korea*

[2]*Silicon Mitus, Korea*

[3]*Samsung Electronics, Korea*

Special Sessions (TUESDAY, OCTOBER 14)

SS6 Neural Modeling, AI Techniques, and Nonlinear Circuits in Emerging Technologies

Organizers: Yoko Uwate (Tokusima University, Japan)

Chair: Yoko Uwate (Tokusima University, Japan)

9:00~10:30, TUESDAY_OCTOBER 14, 2025

CAPRI (2F)

SS6-1 (60)
9:00-9:15

FaceLiVT: Energy Efficient Face Recognition With Linear Vision Transformer For Limited Resource Device

Novendra Setyawan[1,3], Jun-Xian Gu[1], Chi-Chia Sun[2], Mao-Hsiu Hsu[1], Wen-Kai Kuo[1], Chung-An Shen[4], and Jun-Wei Hsieh[5]
[1]National Formosa University, Taiwan
[2]National Taipei University, Taiwan
[3]University of Muhammadiyah Malang, Indonesia
[4]National Taiwan University of Science, Taiwan
[5]National Yang Ming Chiao Tung University, Taiwan

SS6-2 (74)
9:15-9:30

Design of Dual-frequency Load-Independent Class-E Inverter

Yinchen Xie[1], Wenqi Zhu[2], Yutaro Komiyama[1], Ayano Komanaka[1], Akihiro Konishi[3], Kien Nguyen[1], and Hiroo Sekiya[1]
[1]Chiba University, Japan
[2]Tokyo University of Science, Japan
[3]Sojo University, Japan

SS6-3 (81)
9:30-9:45

Mask 3D Parameter Prediction in EUV Lithography by Convolutional Neural Network

Atsushi Takahashi, Moe Sugiyama, Masayuki Shimoda, and Hiroyoshi Tanabe
Institute of Science Tokyo, Japan

SS6-4 (173)
9:45-10:00

Inter-spike interval analysis of a spiking neuron reduced to piecewise-constant dynamics

Yuta Morimitsu, and Tadashi Tsubone
Nagaoka University of Technology, Japan

SS6-5 (202)
10:00-10:15

Time-Evolving Bifurcation Phenomena in a Chaotic Circuit with a Memristor

Taishi Segawa, Yoko Uwate, and Yoshifumi Nishio
Tokushima University, Japan

SS6-6 (261)
10:15-10:30

An experiment of neural prosthesis based on an electronic circuit spiking neuron model

Shogo Shirafuji, and Hiroyuki Torikai
Hosei University, Japan

SS7 Wearable Circuits & Systems for Quality-of-Life: Innovations in GeronCAS

Organizers: Fakhrul Zaman Rokhani (University Putra Malaysia, Malaysia)

Chair: Fakhrul Zaman Rokhani (University Putra Malaysia, Malaysia)

9:00~10:30, TUESDAY_OCTOBER 14, 2025

SICILY (1F)

SS7-1 (132)
9:00-9:15

Dual-Channel Potentiostat for Electrochemical Measurements with Approximations

Kevin Reagen S.[1], Isa Anshori[1], Infall Syafalni[1,2], Nur Ahmadi[1], Fakhrul Zaman Rokhani[3], Tutun Juhana[1], and Trio Adiono[1]
[1]*Institute of Technology Bandung, Indonesia*
[2]*The University of Tokyo, Japan*
[3]*University Putra Malaysia, Malaysia*

SS7-2 (209)
9:15-9:30

Development of a Knee Rehabilitation Device in Compliance with Medical Device Standard ISO 13485

Kiattisak Sengchuai[1], Watcharin Tayati[2], Dujdow Buranapanichkit[1], Apidet Booranawong[1], and Nattha Jindapetch[1]
[1]*Prince of Songkla University, Thailand*
[2]*Trang Hospital, Thailand*

SS7-3 (219)
9:30-9:45

IoT-Based Elderly Health Management System

Mohd Nazim Mohtar, Siti Anom Ahmad, and Fakhrul Zaman Rokhani
Universiti Putra Malaysia, Malaysia

SS7-4 (229)
9:45-10:00

A 1D SqueezeNet-Based Edge Computing System for Arrhythmia Classification in the Elderly

Feng Jiang[1], Yang Wei Lim[1], Siti Anom Ahmad[1], Faisul Arif Ahmad[1], Luthffi Idzhar Ismail[1], Ahmed Faeq Hussein[2], and Fakhrul Zaman Rokhani[1]
[1]*University Putra Malaysia, Malaysia*
[2]*Al-Nahrain University, Iraq*

SS7-5 (242)
10:00-10:15

Development of Drowsiness Detection in Elderly Drivers Using an AI Chip

Asavaron Limsuebchuea, Rakkrit Duangsoithong, and Nattha Jindapetch
Prince of Songkla University, Thailand

SS7-6 (277)
10:15-10:30

A Multichannel Photoplethysmography Pipeline with Signal Quality Assessment for Robust Respiratory Rate Estimation

Jeffrey Chow, Nur Ahmadi, Trio Adiono, and Fariska Zakhralativa Ruskanda
Bandung Institute of Technology, Indonesia

SS8 Energy-Efficient Hardware Architectures for Advanced Edge Computing Applications

Organizers: Yuan-Ho Chen (National Taiwan University of Science and Technology, Taiwan)

Chair: Shin-Chi Lai (National Formosa University, Taiwan)

13:30~14:45, TUESDAY_OCTOBER 14, 2025
SICILY (1F)

SS8-1 (21)
13:30-13:45

Efficient Hardware Architecture for SHA3 Hash Function Implementation in CRYSTALS-Kyber Encryption

Tz-Jen Lin[1], Chang-Jun Lin[1], Hsiu-Wei Chen[1], Shih-Hsu Huang[1], and Po-Yuan Chen[2]
[1]*Chung Yuan Christian University, Taiwan*
[2]*Industrial Technology Research Institute, Taiwan*

SS8-2 (54)
13:45-14:00

Innovative Strategies for Siamese Network Optimization: Leveraging Multi-Level Mask Guidance in Visual Object Tracking

Bo-han Chen, Min-yu Chai, and Chai-chi Tsai
National Cheng Kung University, Taiwan

SS8-3 (299)
14:00-14:15

A Visualization-Assisted Insect Classification Human–Machine Interface System Based on Spatial Pyramid Pooling CNN

Song-Min Ke, Chang-Yu Wu, Chang-Yi Chu, Hoh-Siang Liao, Ying-Hsiu Hung, and Shin-Chi Lai
National Formosa University, Taiwan

SS8-4 (304)
14:15-14:30

A High Energy and Area Efficiency DCIM with Dual-Layer 2-Transistor Approximate Compressor

Ching-Yu Chen, Wei-Chih Ho, and I-Chyn Wey
Chang Gung University, Taiwan

SS8-5 (336)
14:30-14:45

A simple control strategy for achieving Steady-state Current Balance in a Three-arm Series Capacitor Step-down DC-DC Converter

Chen-Tung Hsiao[1,2], Chung-Yi Li[1], Chin Hsia[1], Teo Tee Hui[2], and Chia-Chen Shen[1]
[1]*Chang Gung University, Taiwan*
[2]*Singapore University of Technology and Design, Singapore*

SS9 Recent Advances and Design Trends in Power Management ICs

Organizers: Sung-Wan Hong (Sogang University, Korea)

Chair: Sung-Wan Hong (Sogang University, Korea)

15:00~16:15, TUESDAY_OCTOBER 14, 2025

SICILY (1F)

SS9-1 (39) 15:00-15:15

Triple-source Ground-symmetric Pile-up Resonant Energy Harvester

Joo-Mi Cho, and Sung-Wan Hong
Sogang University, Korea

SS9-2 (77) 15:15-15:30

High-Efficiency Switching Battery Charger for Compact Electronics

Yunho Lee, Hyunjun Park, Minsu Kim, Changwook Ahn, Jihwan Choi, and Hyung-Min Lee
Korea University, Korea

SS9-3 (124) 15:30-15:45

A Galvanically Isolated High Speed Switching Gate Driver for Low-to-Medium Voltage Wide-bandgap Semiconductor

Sangin Choi[1], Hyunuk Jeong[2], Seunghoon Lee[1], Jaemin Kim[3], Chanjung Park[1], Wookang Jin[4], Jaewoon Kim[5], Jinhwan Kim[5], and Kunhee Cho[1]
[1]Sungkyunkwan University, Korea
[2]Kyungpook National University, Korea
[3]NXP Semiconductor, Korea
[4]ON Semiconductor, USA
[5]Samsung Electronics, Korea

SS9-4 (146) 15:45-16:00

Towards a Compact and Power-efficient Pulse-Based Li-ion Battery Charging System with Load Supply Using a Photovoltaic Source

Minsoo Song, and Byunghun Lee
Hanyang University, Korea

SS9-5 (265) 16:00-16:15

Lightweight Power-Management Countermeasures Against Side-Channel Attacks

Yeseul Song, Ayeon Gwon, and Junwon Jeong
Sookmyung Women's University, Korea

Poster Session 1 (MONDAY, OCTOBER 13)

Poster Session

Chair: Youngmin Kim (Hongik University, Korea)

Standing Time 14:45~15:00 & 16:15~16:30, MONDAY, OCTOBER 13, 2025

Exhibition Time 9:30~17:45, MONDAY, OCTOBER 13, 2025

SYDNEY1+2(2F)

Analog and Mixed Signal Circuits and Systems

PS-1 (13) **0.3V Specification-oriented Inverter-based OTAs with NAND-and-NOR CMFB using Different Standard Cells' Strength**

Ngo-Doanh Nguyen[1,2], Duy-Hieu Bui[2], Xuan-Tu Tran[2], and Orazio Aiello[1]
[1]*University of Genoa, Italy*
[2]*Vietnam National University, Vietnam*

PS-2 (34) **A 14-Bit Two Steps 50MS/s SAR-ADC based on Time-Domain Quantization Utilizing High Linearity VTC Method**

Bo Song, Yiyao Xiang, and Mingsheng Xu
Zhejiang University, China

PS-3 (43) **A Sturdy MASH Third-Order Noise-Shaping SAR ADC with Reuse of the SAR ADC**

Jang-hyeon Cho, and Sang-Gyu Park
Hanyang University, Korea

PS-4 (84) **Sparsity and Autocorrelation Peak Difference Based Joint Noise Level and Blur Extent Estimation**

Yu-Chieh Yu, Kuan-Lin Chen, and Jian-Jiun Ding
National Taiwan University, Taiwan

PS-5 (114) **Performance Evaluation and Optimization of the Sampling Process of an Neuropredictive SAR ADC**

Alexander Spielberger[1], Lucas Spitzkopf[1], Albert-Marcel Schrotz[1], Christof Pfannenmuller[2], Robert Weigel[1], and Norman Franchi[1]
[1]*Universitat Erlangen-Nurnberg, Germany*
[2]*Otto von Guericke University Magdeburg, Germany*

PS-6 (130) **Analog Blocks for 8-bit SAR ADC: Rail-to-Rail Comparator and Two-Stage Operational Amplifier Designed with Open-Source Tools and Sky130 PDK**

Uriel Jaramillo-Toral[1], Susana Ortega-Cisneros[1], Emilio Isaac Baungarten-Leon[1,2], Erick Jaramillo-Toral[3], and Hector Emmanuel Munoz Zapata[1]
[1]*Centro de Investigacion y de Estudios Avanzados del Instituto Politecnico Nacional, Mexico*
[2]*Universidad Autonoma de Guadalajara, Mexico*
[3]*Instituto Tecnol´ogico de Aguascalientes, Mexico*

PS-7 (192) **Design Considerations for a Third Order Passive Loop Filter in a PLL**

Asif Rahman, and Chithra
Indian Institute of Technology Kanpur, India

PS-8 (214) **A Derivative-Sign Discrimination Based Calibration Scheme for Timing Skew in Dual-channel TIADCs**

Xin Li, Mengdi Miao, Ying Pan, Yu Liu, Chenghu Dai, Yongliang Zhou, Xiulong Wu, and Zhiting Lin
Anhui University, China

PS-9 (226) **Design of Low-Spur Sub-Sampling PLL Employing a Passive Gain-Boosting Isolated SSPD**

Yanlong Cai, Wenhui Liao, Yao Jiang, Ke Chen, Bi Wu, and Chenggang Yan
Nanjing University of Aeronautics and Astronautics, China

PS-10 (238) **A Study on the Very Small Phase Difference Measurement Circuit Suitable for Integration of Multi-Point Phase Difference Measurement System**

Maa Shimogawa, Takuro Noguchi, Akio Shimizu, and Yohei Ishikawa
National Institute of Technology, Ariake College, Japan

PS-11 (247) **A Low-Voltage DTMOS-Based Grounded Synthetic Inductor Using MOS-C Technique**

Ruchita Gupta, Bhawna Aggarwal, and Maneesha Gupta
Netaji Subhas University of Technology, India

PS-12 (270) **A Low-power Open-Loop Spread-Spectrum Clock Generator Design for Ref-Clk Applications**

Yuxiao Zhang[1], Ziwang Cao[1], Yejuan Zeng[2], Xu Meng[1], and Yongsheng Yin[1]
[1]*Hefei University of Technology, China*
[2]*Anhui University, China*

PS-13 (271) **A Low-Power PLL with Supply Noise Insensitive VCO in 65nm CMOS**

Thinh Tran-Dinh[1], Minh Nguyen-Quang[2], Hung Le-Quang[2], Du Doan-Khanh[2], Huy Do-Quang[2], Sang-Gug Lee[1], and Loan Pham-Nguyen[2]
[1]*Korea Advanced Institute of Science and Technology, Korea*
[2]*Hanoi University of Science and Technology, Vietnam*

PS-14 (274) **A Capacitor-less LDO with enhanced Wide Band Power Supply Rejection for Voltage-Controlled Oscillator**

Chengcheng Zhou, Jiawen Yang, Rui Li, Yongsheng Yin, and Xu Meng
Hefei University of Technology, China

PS-15 (288) **A Low-Power Bidirectional Clamping Circuit Using Current-Starved Inverter and Current Mirror**

Narala Venkateswarlu, and Gajendranath Chowdary
Indian Institute of Technology, India

Artificial Intelligence Circuits, Systems, and Applications

PS-16 (3) **A Wide Bandwidth TIA with Low Power Consumption for PNN Prototyping**

L S S Pavan Kumar Chodisetti, Jen-Yu Li, Pradyumna Vellanki, Yung-Jr Hung, and Chua-Chin Wang
National Sun Yat-sen University, Taiwan

PS-17 (25) **RoPE on the Fast Track: Latency-Optimized LLM Inference on GPUs with Low-Rank QKV factorization and Rotary Positional Embedding**

Gilhyeon Lee, Jihoon Jang, Kyungmin Goh, and Hyun Kim
Seoul National University of Science and Technology, Korea

PS-18 (27) **Efficient MXINT4 Inference via Hardware Based Dynamic Sparsity Detection and Skip Activation**

Youngchan Kim, and Hyun Kim
Seoul National University of Science and Technology, Korea

PS-19 (35) **Neural-Network-Based Forward-Backward Equalizer for PAM4 Wireline Communication**

Hanseok Kim[1,2], Yoona Lee[1], Jae Hyung Ju[3], Sihyun Lee[1], Kahyun Kim[1], and Woo-Seok Choi[1]
[1]Seoul National University, Korea
[2]Samsung Electronics, Korea
[3]Georgia Institute of Technology, USA

PS-20 (40) **A NOR8T SRAM Digital Compute-in-memory Macro for Sparse and Scalable edge-AI Processing**

Pratham Sharma[1], Mukul Lokhande[1], Akash Sankhe[1], Kwok Tai Chui[2], Brij Bhooshan Gupta[3], and Santosh Kumar Vishvakarma[1]
[1]Indian Institute of Technology Indore, India
[2]Hong Kong Metropolitan University, Hong Kong
[3]Asia University, Taiwan

PS-21 (47) **An Energy-Efficient Vision Language Model Inference with Importance-aware Token Pruning**

Zhamaliddin Kalzhan, Songyeon Hong, and Hoi-Jun Yoo
Korea Advanced Institute of Science and Technology, Korea

PS-22 (78) **A new narrowband active noise control system with improved applicability**

N. Hara[1], Y. Xiao[1], T. Shirakawa[1], Y. Ma[2], L. Ma[3], and K. Khorasani[3]
[1]Prefectural University of Hiroshima, Japan
[2]Jiangnan University, China
[3]Concordia University, Canada

PS-23 (144) **ReNoC-ML: Reliability-Aware Network-on-Chip Performance Modeling using Machine Learning**

Zhuofan Lin[1], Yang Wei Lim[1], Yongfu Li[2], and Fakhrul Zaman Rokhani[1]
[1]*University Putra Malaysia, Malaysia*
[2]*Shanghai Jiao Tong University, China*

PS-24 (170) **Memory and Energy Savings in the FPGA Implementation of Keyword Spotting with Stream Processing**

Yuto Tada[1], Masanori Hashimoto[2], Makoto Miyamura[3], Xu Bai[3], Toshitsugu Sakamoto[3], and Hiroyuki Ochi[1]
[1]*Ritsumeikan University, Japan*
[2]*Kyoto University, Japan*
[3]*NanoBridge Semiconductor, Inc., Japan*

PS-25 (184) **Pose-Based Video Sign Language Recognition on Edge Devices using Deep Neural Networks**

Erik Tang
La Jolla Country Day School, USA

PS-26 (191) **RecFlash: Fast Recommendation Inference on NAND Flash-Based In-Storage Computing with Embedding-Optimized Data Mapping**

Jangho Baik[1], Gisan Ji[1], Wonbo Shim[2], and Sungju Ryu[1]
[1]*Sogang University, Korea*
[2]*Seoul National University of Science and Technology, Korea*

PS-27 (225) **Lightweight Distil-Whisper and Hardware-efficient FPGA Acceleration for Edge ASR**

Yijing Yang, Xuenan Wang, Bi Wu, Chenggang Yan, and Ke Chen
Nanjing University of Aeronautics and Astronautics, China

PS-28 (232) **Cuffless Blood Pressure Estimation Using Wearable Devices Based on Attention Mechanisms and Synthetic Data from Generative Models**

Che-An Chen[1], Chuan-En Chou[1], Pei-Yun Tsai[2], and Tzung-Dau Wang[3]
[1]*National Central University, Taiwan*
[2]*National Taiwan University, Taiwan*
[3]*National Taiwan University Hospital, Taiwan*

PS-29 (256) **Improvement of A2C Training Efficiency with FSM-based Meta-Optimizer on CPU-FPGA Platform**

Chavakorn SOMJAISUK, and Yukio MITSUYAMA
Kochi University of Technology, Japan

PS-30 (287) **FOSCU: Feasibility of Synthetic MRI Generation via Duo-Diffusion Models for Enhancement of 3D U-Nets in Hepatic Segmentation**

Youngung Han[1], Kyeonghun Kim[2], Seoyoung Ju[3], Yeonju Jean[4], Minkyung Cha[1], Seohyoung Park[4], Hyeonseok Jung[5], Nam-Joon Kim[1], Woo Kyoung Jeong[6], Ken Ying-Kai Liao[7], and Hyuk-Jae Lee[1]
[1]*Seoul National University, Korea*
[2]*OUTTA, Korea*
[3]*Sangmyung University, Korea*
[4]*Ewha Womans University, Korea*
[5]*Chung-Ang University, Korea*
[6]*Sungkyunkwan University School of Medicine, Korea*
[7]*NVIDIA, USA*

PS-31 (289) **System-on-Chip Implementation of Deep Learning RF Fingerprinting for Device Authentication**

Duc Dung Vu[1], Vu Hoang Thang Chau[1], Ivan Schipper[1], Mateo Favel[2], Muhammad Asad Imran Rafique[1], Bo Li[1], and Ediz Cetin[1]
[1]*Macquarie University, Australia*
[2]*Polytech Paris-Saclay University, France*

PS-32 (306) **Progressive NAS for Efficient Structural Pruning of Pretrained Language Models**

Amrita Rana, and Kyung Ki Kim
Daegu University, Korea

Sensory Circuits and Systems

PS-33 (136) **Battery-Less and Sensor-Less LoRa Node for Water Turbidity Monitoring**

Arvin Raj Ramesh[1], Samsuzana Abd Aziz[1], Norulhuda Mohamed Ramli[1], Khairudin Nurulhuda[1], Roberto La Rosa[2], Orazio Aiello[3], and Fakhrul Zaman Rokhani[1]
[1]*University Putra Malaysia, Malaysia*
[2]*STMicroelectronics, Italy*
[3]*University of Genoa, Italy*

Poster Sessions 2 (TUESDAY, OCTOBER 14)

Poster Session

Chair: Youngmin Kim (Hongik University, Korea)

Standing Time 14:45~15:00 & 16:15~16:30, TUESDAY, OCTOBER 14, 2025

Exhibition Time 9:30~17:45, TUESDAY, OCTOBER 14, 2025

SYDNEY1+2(2F)

Beyond CMOS: Nanoelectronics and Hybrid Systems Integration

PS-34 (260) **2D Material Characterisation Using In-Memory Predictive Analytics**

Kishan Kartha, Aleena Kabeer, and Alex James

PS-35 (285) **Novel 4T-2C Ferroelectric Non-Volatile Memory Cell Featuring Non-Destructive Read**

Nihal Raut, Harshitha Gangu, Vatika Jhanjee, Abhishek Kadam, and Veeresh Deshpande
Indian Institute of Technology Bombay, India

Biomedical Circuits and Systems

PS-36 (102) **An Ultra-High-Frequency Neural Stimulator Design Compatible for both 3.3-V and 30-V Output**

Ziyue Wu, and Xu Liu
Beijing University of Technology, China

PS-37 (107) **Flow-based Compact Droplet Routing Algorithm for MEDA-Based DMFB**

Emuun Purevdagva, Masayuki Shimoda, Satoshi Tayu, and Atsushi Takahashi
Institute of Science Tokyo, Japan

PS-38 (284) **A Comparative Study of Adaptive Channel Selection for Resource-Constrained On-Chip Seizure Detection**

Shanmugam S, Ankur Gupta, and Laxmeesha Somappa
Indian Institute of Technology Bombay, India

PS-39 (295) **Poincaré Embeddings for Brain Age Estimation and Hierarchical Biomarker Discovery**

Seung Woo Heo, Nam Jun Kim, and Hyuk Jae Lee
Seoul National University, Korea

Digital Integrated Circuits and Systems

PS-40 (10) **FCP-LLM: Functional Coverpoint Plan Generation Using LLM in Early Design Verification Stage**

Zhuofan Lin[1,2], Zixian Guo[1,2], Chao Wang[1], Ruixin Zheng[1], Yuxin Ji[1], Yang Wei Lim[2], Yuhang Zhang[1], Fakhrul Zaman Rokhani[2], and Yongfu Li[1]
[1]*Shanghai Jiao Tong University, China*
[2]*University Putra Malaysia, Malaysia*

PS-41 (53) **Alt-FF: A Logic-Level Design of Flip-Flop Control for Side-Channel Protection**

Manami Nishimura[1], Tomoaki Ukezono[2], and Toshinori Sato[1]
[1]*Fukuoka University, Japan*
[2]*Kindai University, Japan*

PS-42 (63) **Highly-Efficient Unified Polynomial Arithmetic Module Architecture for Falcon PQC Scheme**

Quang Dang Truong[1], Tuy Tan Nguyen[2], and Hanho Lee[1]
[1]*Inha University, Korea*
[2]*Florida State University, USA*

PS-43 (92) **High-Speed Matrix-Thread Co-Optimized NTT Design for ML-KEM**

Gong Chen[1], Jiansheng Chen[1], Tianyang Yu[1], Zhirui Zhang[1], Bei Wang1, Fangyu Zheng[2], and Yijun Cui[1]
[1]*Nanjing University of Aeronautics and Astronautics, China*
[2]*University of Chinese Academy of Sciences, China*

PS-44 (100) **An IREE Compiler-Based SoC Design for Efficient On-Device AI Inference Acceleration**

Suhwan Park[1], Sangcheol Park[1], Jin-Ku Kang[1], and Yongwoo Kim[2]
[1]*Inha University, Korea*
[2]*Korea National University of Education, Korea*

PS-45 (101) **Efficient FPGA Implementation of Compressor Trees Based on Generalized Paralell Counter Chains**

Mugi Noda, and Nagisa Ishiura
Kwansei Gakuin University, Japan

PS-46 (111) **A 28nm Floating-Point SRAM-based CIM Macro With Shifting-in-memory Exponent Normalization and Mantissa Alignment**

Zhiting Lin, Yang Yang, Miao Long, Hao Li, Rongtao Li, Wenqiang Zhang, Xin Wang, Qiang Zhao, Xiulong Wu, and Yu Liu
Anhui University, China

PS-47 (175) **RNS Base Conversion Using Optimized Multiword Multipliers for Approximate Modulus Switching**

Muhammad Ogin Hasanuddin, and Hanho Lee
Inha University, Korea

PS-48 (181) **Comparison of Barrett Modular Reduction with Various Multipliers in the Context of BFV/BGV Homomorphic Encryption**

Muhammad Daffa Rasyid, Ardianto Satriawan, and Hanho Lee
Inha University, Korea

PS-49 (196) **FPGA-Based Real-Time ISP Accelerator Using Low-Cost Line Buffers and Non-Linear Functions**

Seungwoo Hong[1], Jung Gyu Min[1], Jin Hyun[1], Jaehee Kim[1], Dongyun Kam[1], Eunji Yoo[1], Pilsu Kim[2], Jaehyung Yoo[2], Hyong-Euk Lee[2], and Youngjoo Lee[3]
[1]*Pohang University of Science and Technology, Korea*
[2]*Samsung Advanced Institute of Technology, Korea*
[3]*Korea Advanced Institute of Science and Technology, Korea*

PS-50 (212) **A Simulation-based Study on Impact of DVS for Side-channel Attacks**

Ryoma Katsube[1], Shinichi Nishizawa[2], Toshinori Sato[1], and Tomoaki Ukezono[3]
[1]*Fukuoka University, Japan*
[2]*Hiroshima University, Japan*
[3]*Kindai University, Japan*

PS-51 (227) **Experimental Analysis of Quantum Annealing for Satisfiability Problems**

Remma Ukaku[1], Tomohisa Kawakami[2], and Hiroyuki Tomiyama[1]
[1]*Ritsumeikan University, Japan*
[2]*Duke University, USA*

PS-52 (240) **On the Hardware Efficiency of Short-Length Polarization-Adjusted Convolutional Polar Decoders**

Junehyuk Oh[1], Soonhyun Kwon[1], Dongyun Kam[1], and Youngjoo Lee[2]
[1]*Pohang University of Science and Technology, Korea*
[2]*Korea Advanced Institute of Science and Technology, Korea*

PS-53 (255) **Dual-Clock Optimization for Multi-Core Base Conversion in Fully Homomorphic CKKS Scheme**

Rafael Aditya Cahyo W.[1], Handy Jonarta[1], Muhammad Ogin Hasanuddin[1], Infall Syafalni[1,2], Nana Sutisna[1], and Trio Adiono[1]

PS-54 (269) **CIPHERX: A Unified High-Efficiency AES Encryption and CMAC Authentication Accelerator for Edge Applications**

Sreyas Janamanchi, Pradyumna G, Chinmay Krishna R, and Madhav Rao
International Institute of Information Technology Bangalore, India

PS-55 (305) **Performance Evaluation of Adaptive Stochastic Computing Based Image Processing Approaches**

Keerthana Pamidimukkala[1], Kyung Ki Kim[2], Yong-Bin Kim[3], and Minsu Choi[1]
[1]*Missouri University of Science and Technology, USA*
[2]*Daegu University, Korea*
[3]*Northeastern University, USA*

PS-56 (307) **Sparsity-Gated FP16 MAC Pipeline for Energy-Efficient eDRAM-Based Neural Inference**

Akshay Kumar Sharma, and Kyung Ki Kim
Daegu University, Korea

Neural and Nonlinear Circuits and Systems

PS-57 (51) **Rigorous Verification of implicit Poincare Map Generated by a Sinusoidally forced Continuous Piecewise Linear Circuit**

Hideaki Okazaki, and Naohiko Inaba
Shonan Institute of Technology, Japan

PS-58 (272) **N-coupled CMOS Differential Relaxation Oscillators for Deep Oscillatory Neural Networks**

Kunjeti Dharanidhar Gupta, Srinivasa Chakravarthy, and Sankaran Aniruddhan
Indian Institute of Technology Madras, India

Power and Energy Circuits and Systems

PS-59 (20) **Nanomechanical Self-Timed Power Management Circuit for Low-Power IoT Devices**

Guangwei Liao, Roshan Weerasekera, and Dinesh Pamunuwa
University of Bristol, United Kingdom

PS-60 (233) **A Fully-Integrated LDO with High PSR and Fast Transient Response Using Adaptive Feed-Forward Ripple Cancellation Technique**

Pengcheng Wang[1], Renjie Fu[1], Yunqi Yang[1], Yilin Xu[1], Fanxun Cai[1], Wenjie Deng[1], Shixuan Wang[1], Wu Wen[2], Chong Duan[2], and Hui Zhang[1]
[1]*Beihang University, China*
[2]*Beijing Microelectronics Technology institute, China*

PS-61 (268) **Comparison of Switched-Capacitor and low-Q Resonant Switched-Capacitor with High-Density Capacitor in 3-D Packaging**

Du Zhou, and Guigang Cai
Hong Kong University of Science and Technology, China

PS-62 (298) **A Single-Mode Three-Phase Dual-Path Hybrid Buck-Boost Converter with Extended VCR Range and Always-Reduced Conduction Loss**

Xinman Li[1,2], Xiongjie Zhang [1,2], Yang Jiang[1], Yan Lu[3], Rui P. Martins[1], and Pui-In Mak[1]
[1]*University of Macau, China*
[2]*UM Hetao IC Research Institute, China*
[3]*Tsinghua University, China*

RF/Communications Circuits and Systems

PS-63 (12) **An L-Band Dual-Low-Noise-Amplifier Bank IC in 65-nm SOI CMOS With <0.8-dB NF and >20-dB Gain for Advanced GNSS Receiver Front Ends**

Li Dai[1,2], Jin Li[1,2,3], Bo Chen[1,2], Linqian Zhao[1,2], and Tao Yuan[1,2,3]
[1]*Shenzhen University, China*
[2]*Guangdong-Hong Kong Joint Laboratory for Big Data Imaging and Communication, China*
[3]*State Key Laboratory of Millimeter Waves, China*

PS-64 (36) **A 16 Gb/s 48.9 fJ/b PVT-Tolerant Standard-Cell-Based Receiver for AC-Coupled Chiplet Interconnects**

Yuki Mitarai, Mototsugu Hamada, and Atsutake Kosuge
The University of Tokyo, Japan

PS-65 (194) **A 15–20 GHz CMOS Variable-Gain Phase Shifter for UAV Detection Radar Systems**

Haram Park, Mingyu Lee, Eunchae Jo, Hyeonwon Song, Seungchan Lee, and Jinseok Park
Chonnam National University, Korea

PS-66 (275) **Design Automation and Optimization of Frequency Dividers**

Poornishwar M, Inban S, S. Ramprasath, and Sankaran Aniruddhan
Indian Institute of Technology Madras, India

Live Demo (MONDAY, OCTOBER 13)

Live Demonstration

Chair: Jusung Kim (Ewha Womans University, Korea)

Standing Time 09:30~17:30, MONDAY, OCTOBER 13, 2025
Exhibition Time 16:30~17:30, TUESDAY, OCTOBER 13, 2025
SICILY (2F)

LD-1

Live Demonstration: FPGA-Based Real-Time ISP Accelerator Using Low-Cost Line Buffers and Non-Linear Functions

Seungwoo Hong[1], Jung Gyu Min[1], Jin Hyun[1], Jaehee Kim[1], Dongyun Kam[1], Eunji Yoo[1], Pilsu Kim[2], Jaehyung Yoo[2], Hyong-Euk Lee[2], and Youngjoo Lee[3]
[1]Pohang University of Science and Technology, Korea
[2]Samsung Advanced Institute of Technology, Korea
[3]Korea Advanced Institute of Science and Technology, Korea

LD-2

Live demonstration: Quickly developed chips with the Agile-Chip Platform

Hideharu Amano, Atsutake Kosuge, Mizuho Nitami, Hirofumi Sumi, Naonobu Shimamoto, Yukinori Ochiai, Yurie Inoue, Tohru Mogami, Yoshio Mita, and Makoto Ikeda
The university of Tokyo, Japan

LD-3

Live Demonstration: ML-KEM PQC Hardware Accelerator for Secure Video Encryption

Yunseong Jang, Seulbee Yang, and Hanho Lee
Inha University, Korea

LD-4

SnuggleSmart: A Wearable Infant Temperature Monitoring System for Real-time Temperature Management and Alerting

Xuya Jiang, Huajie Huang, Changyan Chen, Qing Zhang, Yuhang Zhang, Rui Pan, and Yongfu Li
Shanghai Jiao Tong University, China

LD-5

Live Demonstration: Machine Learning based Dual Direction Prediction Framework for Charge Pump Parameter Optimization

Ashutosh Singh, and Anuj Grover
ECE - IIIT Delhi, India

PrimeAsia (TUESDAY, OCTOBER 14)

PA PrimeAsia

Chair: Jinwook Burm (Sogang University, Korea)

16:30~17:45, TUESDAY_OCTOBER 14, 2025
SICILY (2F)

PA-1
16:30-16:45

Dynamic Performance Enhancement of a Current-Steering DAC Using Tree-Structured Routing and Power Mesh-Based SI/PI Optimization

Min-Jae Seo, In-Ho Jang, and Hyeon-Woo Kim
University of Seoul, Korea

PA-2
16:45-17:00

ML-Pump: A Machine Learning based Bidirectional Prediction Framework for Charge Pump Design Optimization

Ashutosh Singh[1], Anuj Grover[1], and Abhishek Jain[2]
[1]ECE - IIIT Delhi, India *[2]STMicroelectronics, India*

PA-3
17:00-17:15

Development of GNSS Testbed with C/N_0 Simulation Capability

Yongtaek Hwang[1], Jiwoo Hwang[2], and Hoyoung Yoo[1]
[1]Chungnam National University, Korea
[2]Korea Aerospace Research Institute, Korea

PA-4
17:15-17:30

Intelligent Multi Energy Harvesting with GaN device for Smart Home Application

Jongwan Jo[1], Ju Won Oh[1], YoungGun Pu[2], and Kang-Yoon Lee[1]
[1]Sungkyunkwan University, Korea *[2]Skaichips , Korea*

PA-5
17:30-17:45

Energy-Efficient Surveillance via Event-Driven ROI Detection with DVS-CIS Fusion

Mincheol Cha[1,2], Keehyuk Lee[1], Soosung Kim[3], Hyunsurk Ryu[1,3] Xuan Truong Nguyen[1], and Hyuk-Jae Lee[1]
[1]Seoul National University, Korea
[2]HyperAccel Co.,Ltd., Korea
[3]Neuro Reality Vision Corp., Korea

Discussion (WEDNESDAY, OCTOBER 15)

10:00~17:00 WEDNESDAY, OCTOBER 15, 2025

Special Programs

Welcome Reception

Welcome Reception at Paradise Hotel Busan will be provided to **all the on-site registrants** after the Tutorial sessions **on Oct. 12,** respectively.

Date	Sunday, Oct. 12, 2025
Time	18:00-20:00
Venue	SICILY ROOM (1F)

- The venue for the welcome reception is "**SICILY ROOM**", main conference venue.
- Please make sure that you have to show the **Welcome reception coupon in your name badge**. Conference attendee will get a banquet coupon together with the conference admission badge. Please be noted that you have to keep the coupon well and show it to the staff when having Banquet.
- All the conference registration includes an admission ticket for Reception.

Banquet

- **Banquet** at Paradise Hotel Busan will be provided to **all the on-site registrants** after the afternoon sessions **on Oct. 13,** respectively.

Date	Monday, Oct. 13, 2025
Time	18:00-20:00
Venue	Grand Ballroom (2F)

- The venue for the banquet is "**Grand Ballroom**", main conference venue.
- Please make sure that you have to show the **Banquet coupon in your name badge**. Conference attendee will get a banquet coupon together with the conference admission badge. Please be noted that you have to keep the coupon well and show it to the staff when having Banquet.
- All the conference registration includes an admission ticket for banquet.

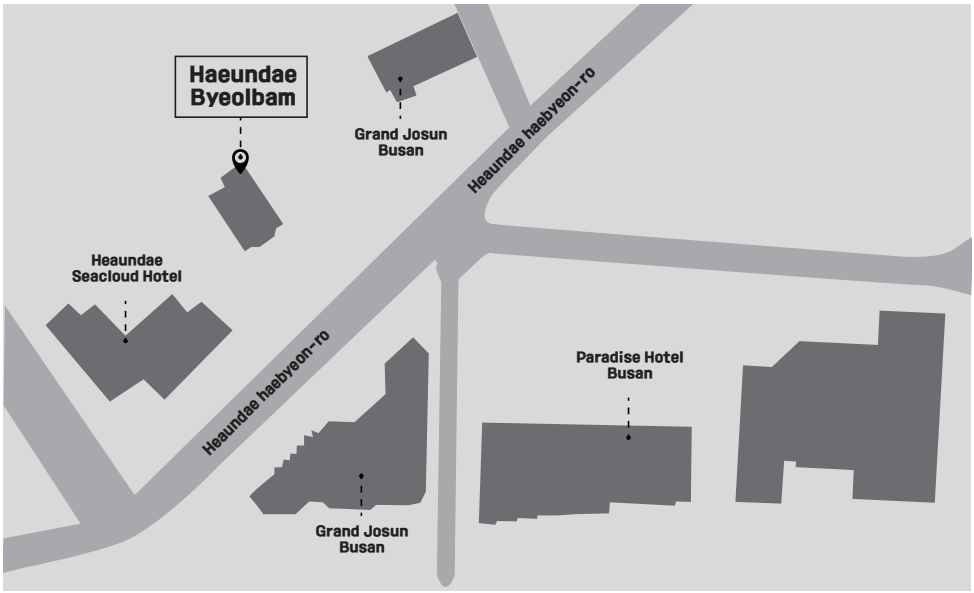
Farewell Reception

- **Farewell Reception** at Haeundae Byeolbam will be provided to **all the on-site registrants** after the afternoon sessions **on Oct. 14,** respectively.

Date	Tuesday, Oct. 14, 2025
Time	18:20-20:30
Venue	Haeundae Byeolbam (2F)

- The venue for the banquet is "**Haeundae Byeolbam (2F)**", main conference venue.
- Please make sure that you have to show the **Farewell Reception coupon in your name badge**. Conference attendee will get a banquet coupon together with the conference admission badge. Please be noted that you have to keep the coupon well and show it to the staff when having Banquet.
- All the conference registration includes an admission ticket for Reception.
- This year, Additional Farewell Reception tickets are not available on site.

MAP : Haeundae Byeolbam



Gift Drawing

• **Gift Drawing** for conference attendants will be held during the **Closing Ceremony.**

Date	Tuesday, Oct. 14, 2025
Time	18:20-20:30 [Farewell Reception]
Venue	Haeundae Byeolbam (2F)

(Sample Image)

Gift Drawing ticket
Don't lose it!

Put on ticket in the box
at Registration desk.

Samsung Galaxybook4

Apple Airpod Max Pro

LG Gram +View

Viewsonic Mini Beam projector

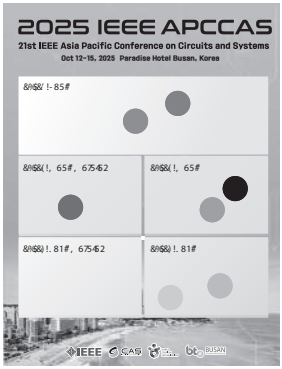
Gift for Session Participants

- A sticker for each attendee will be provided by our session staff at the end of each session including Tutorials, Short Tutorials, and Company Exhibition.
- We present **Special gift** based on the number of stickers. Please do not miss this chance.
- You can receive the **gift at the registration desk.**

Date	Programs	Slot Completion Condition	Gift Claim Condition
Oct. 12 (Sun.)	- Tutorials	More than **2 Stickers for each slot**	Complete more than **3 slots.**
Oct. 13 (Mon.)	- Keynotes Speeches		
	- Afternoon Session-1 - Afternoon Session-2 - Afternoon Session-3		
Oct. 14 (Tue.)	- Morning Session - Keynotes Speeches		
	- Afternoon Session-1 - Afternoon Session-2 - Afternoon Session-3		

*** All stickers must have different colors/shapes.**

*** Gifts are offered on a first-come, first-served basis, so it can be sold out early.**



CONFERENCE INFORMATION

Lunch

- **Lunch** at Paradise Hotel Busan will be provided to **on-site registrants** after the morning sessions **on Oct. 13 and Oct. 14**, respectively.

Date	Monday, Oct. 13, 2025	Tuesday, Oct. 14, 2025
Time	12:20-13:30	
Venue	Grand Ballroom (2F)	Lunch Voucher Redemption: Registration Desk

- PLunch vouchers can be redeemed at the registration desk, and participants will receive meal support to enjoy authentic local cuisine at nearby restaurants in Busan.
- Please make sure to show the lunch coupon included in your name badge.
- Conference attendees will receive the lunch coupon together with the admission badge.
- Please keep the coupon safe and present it to the staff when redeeming.
- Lunch locations may be subject to change. Please refer to the on-site guide for updates.

Coffee Break

- **Coffee and Cookies** will be served at the following hours.

Date	Monday, Oct. 13, 2025		Tuesday, Oct. 14, 2025	
Time	11:20-11:30	14:45-15:00	10:30-10:40	14:45-15:00
Venue	Grand Ballroom Lobby (2F)			

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- If you want to download the file to your USB or external drive, please ask our staffs at the registration desk.

- Please use your PC/MAC/Laptops for full access. (Not Accessible through smartphones)

Emergency Calls

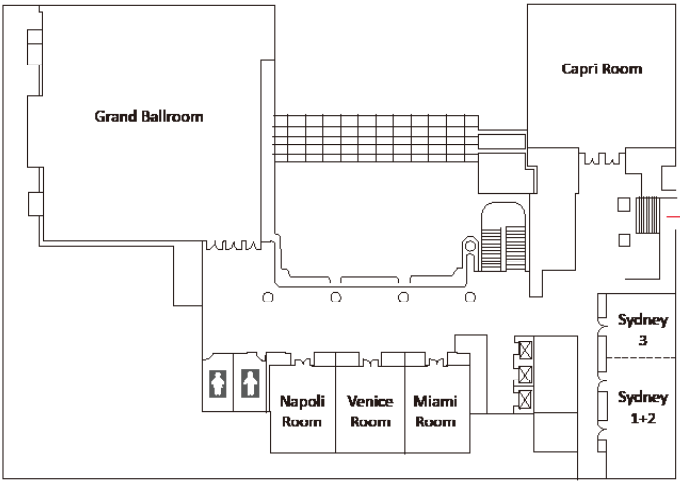
Secretary Chair	Prof. Hyun Kim (Mobile: 010-9600-5427) Prof. Joo-Hyung Chae (Mobile: 010-7203-1216)
Police Services	112
Fire, Rescue & Hospital Services	119
Non-urgent Medical	129
Coast Guard	1339
Disaster Safety Confirmation	1330
Report Child Abuse	112

Venue

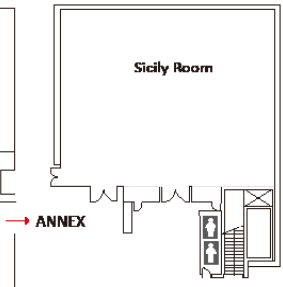
PARADISE
HOTEL BUSAN

- 296, Haeundaehaebyeon-ro (Jung-dong), Haeundae-gu, Busan, Korea
- Website: https://www.busanparadisehotel.co.kr/front
- Tel: +82 51-742-2121
- Fax: +82 51-742-2100

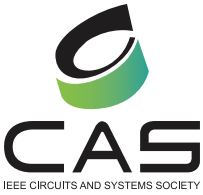
Main Bldg. 2F



Main Bldg. 1F




IEEE


CAS
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Artificial Intelligence (AI) Hardware Center

ASRC

자동차향 시스템반도체 융합인력 육성센터

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AI 반도체 프로세싱 SW 연구센터

AI Semiconductor Processing SW Research Center

대규모데이터센터용
인공지능시스템반도체 연구센터

연구센터 소개

연구명

초거대 AI를 위한 대규모데이터센터용 인공지능 시스템반도체 인력 양성 및 핵심기술 개발

연구내용

- 대규모 네트워크 경량화 및 최적화 설계
- 데이터처리용 전력변환회로 및 인터페이스 설계
- 최적 구조 메모리 어레이 개발
- 저전력 고효율 시냅스 소자 및 구동회로 개발

참여인력

참여 연구자 총 100명

- 대학교수 11명 / 산중교수 1명
- 전임연구원 1명
- 석사 73명 / 박사 14명

참여 대학 4개, 참여 기업 17개

참여 대학

서강대학교 SOGANG UNIVERSITY, 고려대학교 KOREA UNIVERSITY, 서울시립대학교 UNIVERSITY OF SEOUL, 단국대학교 DANKOOK UNIVERSITY

참여 기업

SAMSUNG 삼성전자, SK 하이닉스, LG전자, DB하이텍, SFE (주)에스에프이, LX Semicon, Silicon Mitus, PIXELPLUS, nextchip, SYNOPSYS, Telechips, SAPEON, BYDA, Trans Biolab, TechwidU, 센서위드유, OPENEDGES

연구 개발 및 인력 양성 목표

최종 연구 목표

초거대 AI를 위한 대규모데이터센터에 활용될 수 있는 초고효율 · 초저전력 인공지능 반도체 핵심 기술 개발 및 고급 인력 양성

(수혜인원: 총 600명, 배출인원: 총 480명)

연구센터의 핵심 목표

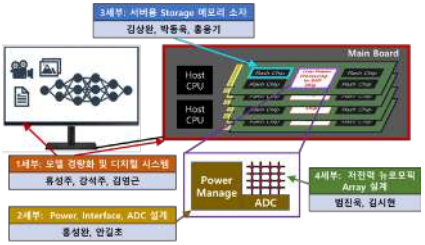
- 인공지능 반도체를 위한 시스템 핵심/응용 SW 기술과 회로/소자 핵심 설계 및 융합 기술 개발
- 초거대 AI를 위한 대규모데이터센터에 활용 가능한 인공지능 반도체 플랫폼 연구 개발
- 인공지능 반도체 관련 소프트웨어와 하드웨어 설계 역량을 갖춘 SW-HW 융합형 석·박사 고급 인력 양성
- 산업체 수요 중심의 실증적 연구와 창의/융합형 인재 육성을 통한 인공지능 반도체 분야의 선도적인 연구센터 운영

주요 연구 내용

- 대규모 멀티모달 네트워크 시스템 경량화 설계 및 최적화
- 대규모서버용 Storage 메모리 소자 개발
- 고효율 전력변환회로/고속 ADC 및 Interface 설계
- 저전력 고효율 시냅스 소자/어레이 개발

세부 연구 개발 목표

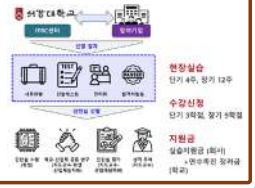
- 데이터센터의 고효율 인공지능 시스템을 위한 Processing-In-SSD SW/HW 플랫폼 설계
- 인공지능시스템을 위한 데이터센터용 고효율 전력변환 및 고속인터페이스 설계기술개발
- 데이터센터를 위한 저전력 차세대 반도체 소자 기술 개발
- 데이터센터용 저전력 고효율 인공지능 연산을 위한 시냅스 어레이 개발



산학밀착형 양방향 인력양성 시스템 구축

산업체 고용연계 추진 계획

산업체 장/단기 인턴쉽 운영



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WE'RE HIRING!

우리는 LLM 서비스에 특화된 고효율 AI 반도체를 개발하며,
기업과 개인이 LLM을 지속적으로 이용할 수 있는 컴퓨팅 인프라를 실현합니다.

신입 / 경력 개발자 채용

접수 방법 : 홈페이지 지원 QR 참조 ↑
근무지 : 강남 뱅뱅 사거리

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아주대학교

지능형 의료 영상 진단 솔루션 연구센터

센터 컨소시엄

지능형 의료 영상 진단 솔루션 연구센터

1세부 지능형 진단 및 AR 기반 시각화 시스템 개발

- 세부책임 | 아주대 선우명훈 교수 — 지능형 진단 딥러닝 최적화 및 연산 엔진 연구
- 서울대 이혁재 교수 — AR 기반 시각화 시스템 개발
- 아주대 박성준 교수 — 피부적합형, 체내 삽입형 전자/광소자 개발
- + 아주대병원 김태희 교수 + 아주대병원 하태양 교수 — 유방암 공동연구
- + 아주대병원 정우영 교수 — 호흡기 질환 공동연구
- NCKU Gwo Giun Lee 교수 — 피부암 검출 및 SoC 연구

2세부 영상/임상 빅데이터 융합 진단 모델 개발

- 세부책임 | 아주대 이정원 교수 — 학습 데이터 품질 기반 진단 모델 검증
- 연세대 고정길 교수 — 학습 기반 의료 영상 분석 시스템 연구
- 포항공대 김원화 교수 — MRI 기반 딥러닝 처리 연구
- + 아주대병원 선주성 교수 — 폐 질환 공동연구
- OUS Mi Zhang 교수 — 의료 데이터 분석 연구

3세부 뇌 영상 및 생체 신호처리 기술 개발

- 세부책임 | 연세대 김동현 교수 — 딥러닝/영상시스템 기반 진단 모델 개발
- 포항공대 이영주 교수 — 생체 신호처리 압축 센싱 복호 기법 연구
- 한국과학기술원 예종철 교수 — 의료영상 처리 연구
- + 서울의료원 최현석 과장 — 뇌 질환 공동연구
- UC 버클리 Chunlei Liu 교수 — 뇌 MRI 진단 연구

혁신도약형과제

4세부 의료용 동적환경 3D 재구성 연구

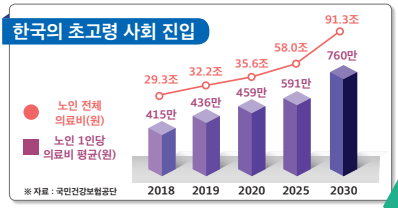
- 세부책임 | 아주대 구형일 교수 — 의료 영상 비강체 3D 재구성 연구
- + 아주대병원 김진홍 교수 + 아주대병원 양민재 교수 — 소화기 질환 공동연구
- 칭화대 Hua Guo 교수 — MRI 영상 재구성 연구

ICT 관련 교수 / 의대 교수 / 해외 대학 교수 / 컨소시엄 기관

에이디테크놀로지	라온텍	인피니트헬스케어	네모누리	딥노이드	자람테크놀로지	제이엘케이	에스앤지바이오텍
ADT	RAONTECH	INFINITT	NEMONURI	DEEP NOID	zaram	JLK	S&G

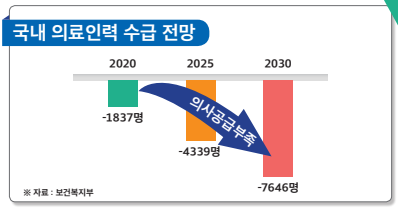
지능형 의료 영상 진단 솔루션 개발

한국의 초고령 사회 진입



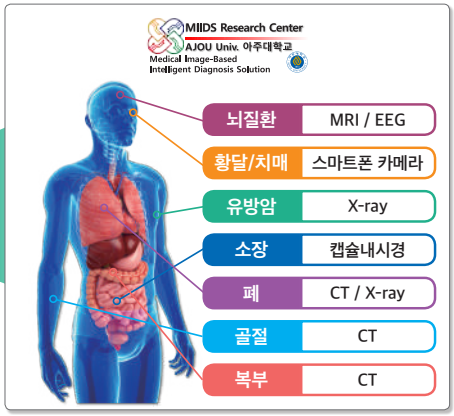
※ 자료 : 국민건강보험공단

국내 의료인력 수급 전망



※ 자료 : 보건복지부

지능형 의료 영상 진단 솔루션



아날로그 RF회로 및 시스템 연구센터

● 센터소개

▶ 본 센터는 EMI/EMC, 밀리미터파 IC 설계, 초고주파 IC 설계, RF 전력증폭기 설계, 전력 IC 설계, 인공지능 IC 설계, 안테나 해석 및 설계 등과 같은 세부 연구분야로 구성

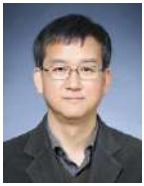
▶ 국내 유일의 고속 IC의 설계 및 시스템의 제작, 그리고 전기장에 대한 노이즈 해석 및 최적화를 단일 센터 내에서 할 수 있는 올인원 시스템을 갖추고 RF 및 고속 시스템 해석을 위한 인프라를 최고로 효율적인 수준으로 유지 관리 하는 것을 목표로 함

● 교수진


서문교 교수


김소영 교수


김병성 교수


나완수 교수


박준은 교수


양영구 교수


이강윤 교수


이우근 교수


박형원 교수

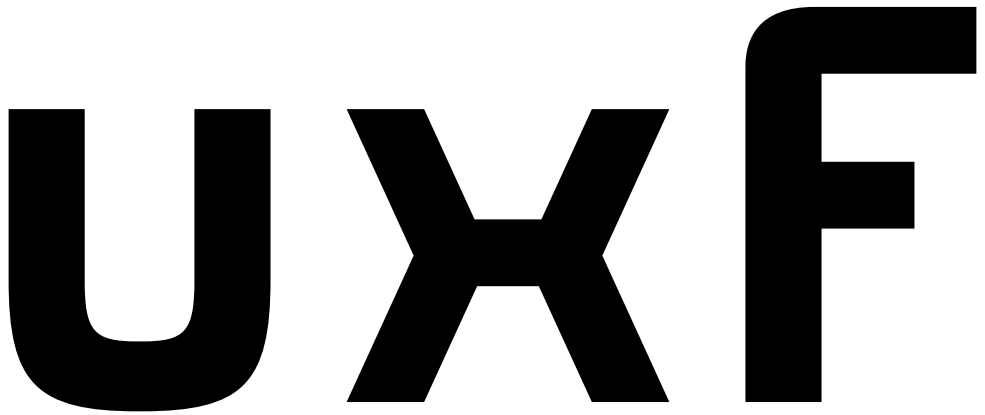

황금철 교수

● Open Lab

http://arrc-skku.co.kr/

성균관대학교 SUNG KYUN KWAN UNIVERSITY(SKKU) | 아날로그 RF회로 및 시스템 연구센터


4lynx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Website

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■ 인테리어 LED Drive

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- 최대 4,076개의 데이지 체인 연결로 통신 링크통합 (시스템비용 절감)
- 자동 온도 보정 및 진단 기능 지원

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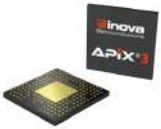
■ ISELED의 통합 연결을 위한 Transceiver

- 하나의 중앙 컨트롤러로 차량 전체 조명제어 가능
  - 자동차 ESD 및 EMC 요구사항을 충족하는 40V 견고한 설계
  - 저전력 모드 및 웨이크업 신호
  - 비차폐 연선 케이블을 통한 LED, 센서, 액츄에이터 하위 시스템 연결에 최적화
  - 외부장치 제어를 위한 3GPIO
- 효율적인 전력 조명 구현을 위한 통합 5V DCDC 컨트롤러가 있는 단일12V 전원 공급장치
- 케이블 연결 길이 최소 ~5M 이상

APiX



■ 기가비트 멀티채널 SerDes

- 최대 12Gbps 비디오 전송지원
- MST(Multi-Stream Transport) 기능 지원
- 100Mbps 이더넷 포함, 직렬 인터페이스 프로토콜 지원
- 케이블 성능 모니터링 및 자가 진단 기능 지원

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- 16 and 32 bit MCU for Automotive
- Supports AUTOSAR for HYUNDAI & KIA
- Wireless charging Transceiver
- Battery charging & Management IC

Geehy

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- BLE SoC (BLE 4.2)
- Automotive General-Purpose
- Industrial Control
- High-end Consumer

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TEL : 031-425-2780 | HP : 010-5501-7896 | E-mail : apollo2@sittech.co.kr

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어보브반도체 채용정보 & 복리후생

모집분야	주요업무	자격요건
MCU반도체 디지털 설계 (신입/경력)	IC top intergration - ARM MCU top intergration 설계 - Verilog HDL coding 및 simulation - Cadence, Synopsys EDA tool 사용 (Incisive, Design Vision Synthesis, STA, ATPG, Formality 등) - FPGA 검증 (Altera, Xilinx, C coding) - 양산 test setup support - 제품 특성 평가 진행	[지원자격] - 학력 및 경력 : 학사 이상 / 직무 관련 업무 경력 5 년 이상 - 전공 : 전기 전자 제어 공학 반도체공학 임베디드 시스템 / 컴퓨터 공학 / 소프트웨어 공학 등 관련 학과 학사 또는 석사 이상 졸업자 - ARM Architecture/AMBA BUS 설계 경력 및 설계 업무 관련 EDA tool 사용 경력 필요 [우대조건] - MCU 설계 경험자 - Soc Test setup 경험자
아날로그 회로 설계 엔지니어_Core IP그룹 (신입)	직접회로설계 분야 · Bandgap Reference(BGR), BMR · LowDrop-out (LDO) · Power on Reset(POR) · Brown-out Detector(BOD) · ADC (SAR / Sigma Delta) · DAC · Opamp/TIA 등등 · Clock generator. · Oscillator · Phase Locked Loop(PLL) · Analog IP etc. Power Circuit 회로 설계 · DC-DC Buck Converter · DC-DC Boost Converter · Charge-pump 그 외 · I/O, ESD PAD 설계	[지원자격] · 필수 사항 : 포트폴리오 / 성적증명서 · 정규직 채용 : 석사 이상 / 학부(2년 경력 이상) · 지원 자격 : Analog 집적회로설계 관련 전공 / 업무 / 경력 · 우대 사항 : 회로설계분야 연구실 경험, 교육 수료 (3개월 이상) [직무 역량] · Analog 회로 설계 경험자 · Cadence tool를 이용한 Analog 회로 설계할 수 있는 능력. · Analog 회로 분석할 수 있는 능력. · Schematic/Layout 설계 가능자 · 측정 장비 사용 경험 [우대조건] · SoC 개발 경험자 · 여러가지 Tool(ADS, EMX Tool 등) 가능자 · 여러 공정 / 낮은 공정 설계 경험자 · 집적회로설계와 RTL 설계 동시 가능자 (PLL/ADC/DAC 등) · 집적회로설계 전공 박사학위 소지자

- 성과보상 인사제도
- 포상제도(우수사원,기술개발 등)
- 장기근속포상
- 스톡옵션 제도
- 장학제도 운영

- 유연한 근무시간(자율근무제)
- 의료비지원(본인,배우자,자녀 등)
- 종합검진 지원
- Refresh휴가(4일 부여)
- 기숙사 운영
- 회사콘도운영

■ 근무지 : 서울시 강남구 영동대로 330 총회회관 6~9층

■ 지원방법 : 이메일 지원→Jonghee.kim@abov.co.kr(자유양식 이력서)

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정품 인증, 개봉 여부 확인이 가능한 스마트 포장, 고객 관계 관리 이를 위한 가장 쉬운 방법

TNP200M®은 브랜드 가치를 보호하고, 디지털화된 정보를 활용해 스마트 물류를 가능하게 하며, 유용한 고객 관리 정보를 제공합니다. 작은 NFC 태그 칩 하나로 이 모든 것을 경험해보세요.

디지털 정품 인증

- NFC 태그의 발급 단계에서 개인 키와 UID를 이용하여 디지털 서명을 생성한 후, 상품 생산 단계에서 이 태그를 부착합니다.
  태그가 부착된 제품은 언제든지 스마트폰에 탭 하면 정품 여부를 확인할 수 있습니다.
- 제품의 개봉 여부를 탐지합니다. 제품 개봉 후 스마트폰을 탭 하면 해당 정보를 확인할 수 있으며, 소비자나 검사자가 제품의 무결성을 입증할 수 있습니다.

공급망 및 재고 관리

- NFC 태그를 부착해 제조, 유통, 보관 단계 등 언제든지 제품을 관리할 수 있습니다.
  클라우드 기반의 데이터 모니터링은 물류 효율성과 보안성을 향상시키며 허가 받지 않은 판매 채널에 제품을 유통하는 것을 어렵게 합니다.
- NFC 태그가 부착된 제품은 재고 가시성을 최적화하여, 항상 제품의 재고 상태를 확인할 수 있으며, 소매업체가 적시에 재고를 보충할 수 있도록 도와줍니다

고객 관리

- 소비자에게 제품 구매 단계별 맞춤 메시지를 표시합니다.
  제품 구매 전 제품 생산지, 사용법 등 유용한 정보, 리뷰가 표시될 수 있으며, 제품 구매 후에는 A/S, 할인쿠폰, 소셜 커뮤니티 링크, 온라인 쇼핑몰 연결 등이 표시될 수 있습니다.
- 이러한 고객 관리를 통해 제품 사용 여부, 개별 선호도 및 브랜드 충성도에 대한 데이터베이스를 확보할 수 있습니다.

[디지털 정품인증]


[공급망 및 재고관리]


[고객관리]

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ULTRON II는 AMD ZYNQ UltraScale+ MPSoC 기반의 **고성능 임베디드 개발 플랫폼**입니다.

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  - ARM Mali-400MP2 GPU
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- Soft error rate analysis
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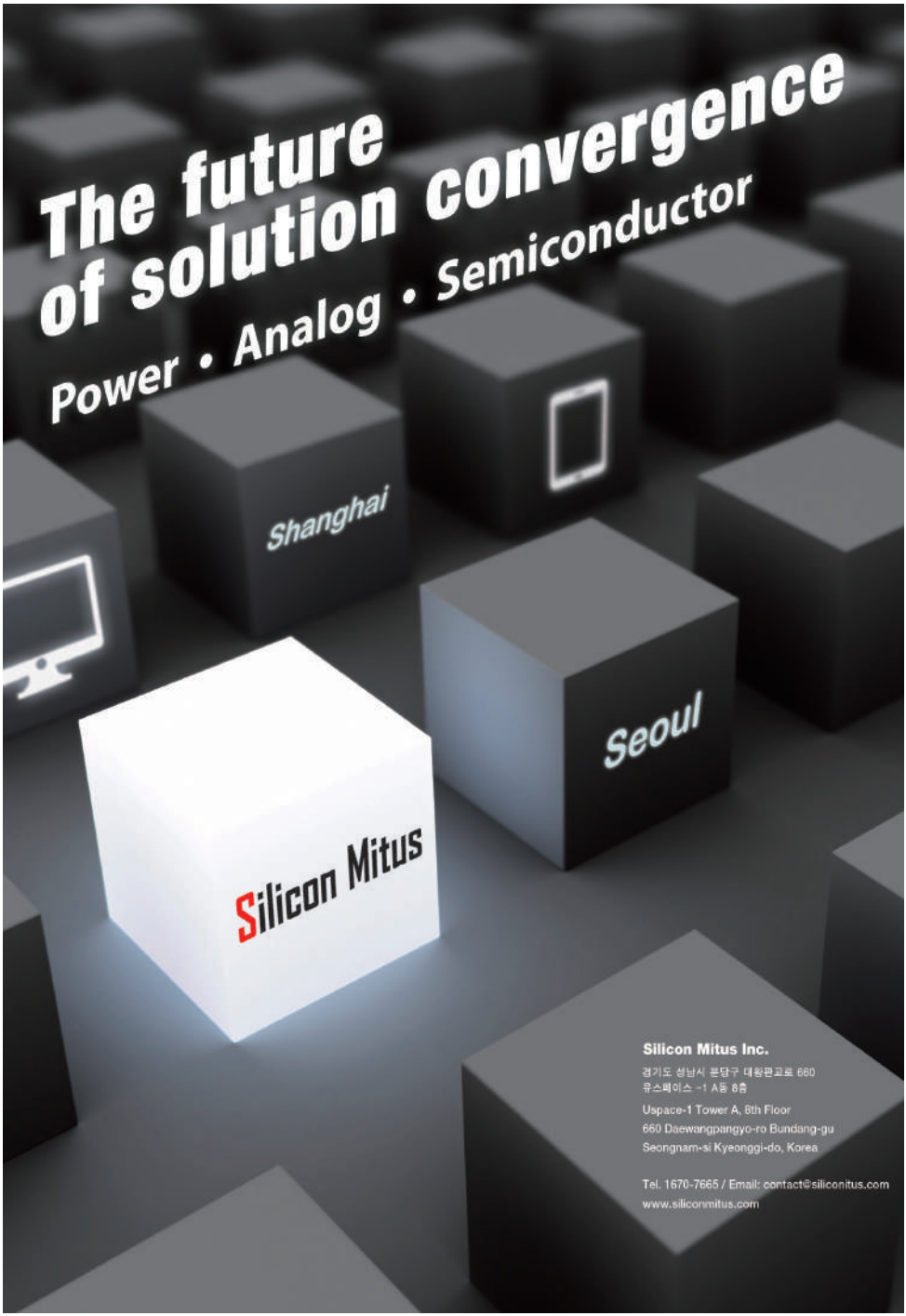

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CIRCLE
Design Solutions

Company Name	CIRCLE Co.,Ltd.
Representative	Jeff Lee
Established	2023.01.10
Location	Pangyo, Seongnam, Gyeonggi

COMPANY HISTORY

2023
Establishment of **CIRCLE Co.,Ltd.**

2024
Relocation of **CIRCLE Co.,Ltd.** Headquarters

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- Implementation PI/PD
- Synthesis to GDS

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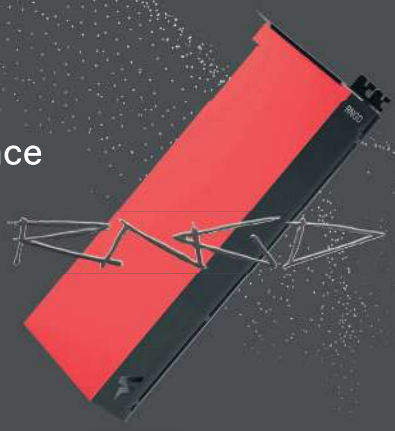

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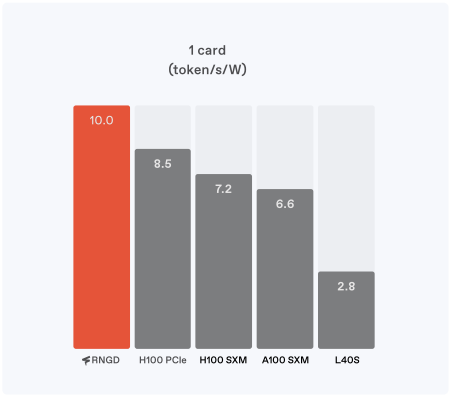

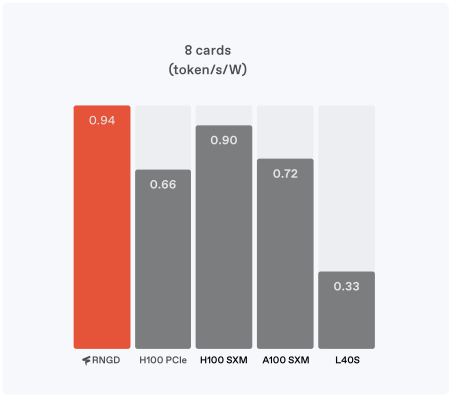

Llama 3.1 8B

8B BF16 | Concurrency 64 | 1024 input / 1024 output tokens

RNGD	Furiosa SDK 25.3.0
H100 PCIe	vLLM 0.9.1
H100 SXM	vLLM 0.9.1
A100 SXM	vLLM 0.9.1
L40S	vLLM 0.9.1

Llama 3.3 70B

BF16 | Concurrency 64 | 1024 input / 1024 output tokens

RNGD	Furiosa SDK 25.3.0
H100 PCIe	1167.1 tokens/s
H100 SXM	vLLM 0.9.1
A100 SXM	vLLM 0.9.1
L40S	vLLM 0.9.1

Disclaimer: RNGD results are based on internal measurements by FuriosaAI using SDK 2025.3.0.
GPU results were obtained using vLLM 0.9.1 on RunPod under comparable test conditions.

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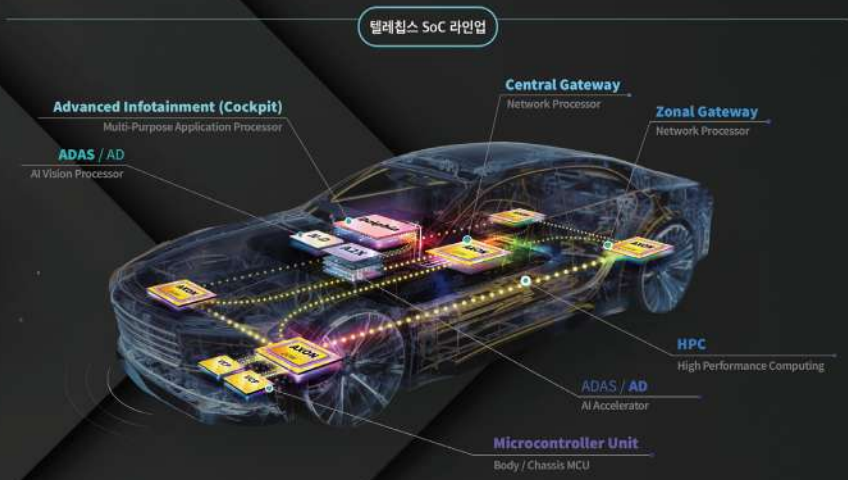
텔레칩스(Telechips)는 자동차 전장 시스템의 핵심 '두뇌' 역할을 수행하는 시스템 반도체 설계 전문 팹리스(Fabless) 기업입니다. SDV(소프트웨어중심차량)로 빠르게 전환되는 산업 트렌드에 발맞춰 텔레칩스는 기존 주력 제품인 차량 인포테인먼트 AP(애플리케이션프로세서)를 중심으로 마이크로컨트롤러유닛(MCU), ADAS(첨단운전자보조시스템), 네트워크 게이트웨이, AI 등 차세대 반도체 라인업을 지속적으로 확대하고 있습니다.



또한, 글로벌 수준의 고성능·저전력 SoC 설계역량과 고객 맞춤형 솔루션을 기반으로 인공지능(AI) 및 자율주행 시장 진입에 속도를 내며 두각을 나타내고 있습니다. 또한, ESG 경영체제 도입과 "고객이 원하는 미래를 위한 새로운 혁신" 이라는 비전 아래 글로벌 파트너들과 함께 더 나은 모빌리티의 내일을 만들어가고 있습니다.

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인공지능(AI) 반도체 IP 플랫폼 전문기업

오픈엣지테크놀로지

세계 유일 AI 반도체의 구동 기반이 되는 통합 IP 솔루션 제공:

1. NPU IP - 인공지능 학습과 실행에 최적화된 신경망 처리장치
2. On-chip Interconnect IP - SoC 내 데이터 이동 통로
3. Memory Controller IP - 스케줄링 알고리즘에 따라 SoC와 DRAM 간 고속 데이터 통신을 제어
4. DDR PHY IP - SoC와 DRAM 간 고속 데이터 전송

반도체 분야 최초 기술평가 AA등급 취득

세계 유일 AI 반도체 통합 IP 솔루션 제공

검증된 글로벌 Track Record

글로벌 기업과의 전략적 파트너십

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채용 공고 확인하기

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테크위드유 주식회사

www.techwidu.com

회사소개

테크위드유 주식회사는 2016년 12월 반도체 개발업, 제조 판매업을 목적으로 설립하여 기술집약적이며, 고품질의 Analog IP 및 제품을 공급하는 국내 Fabless 반도체 설계 회사입니다.
산업용 시스템에서 필요로 하는 고수익 다품종 아날로그 제품 위주로 개발하고 있으며, 부가적으로 초미세 공정향 아날로그 기반 설계기술의 확보를 통해 Analog IP 들을 국내외 고객에게 제공하고 있습니다.

서비스 및 아이템 소개

1) Mixed-signal IP & Platform
   Generic Analog IP (LDO/POR/VLD/ADC 등)
   Power management IP (DC-DC Converter 등)

2) Industrial SoC
   DC Motor Driver IC
   Multi-channel PMIC

3) Automotive SoC
   USB Type-C PD Charger IC
   Head Lamp LED Driver IC

복리후생제도

건강검진 비용 지원 (2인)	선택적 복리후생 (체력단련, 자기개발 등)
식사 및 스낵바 제공	경조사 지원
장기근속 포상 및 휴가 (만 5년↑ 300만원)	콘도 회원권 운영
특허 보상금 (출원 50만원 / 등록 100만원, 200만원)	사내 대출 제도


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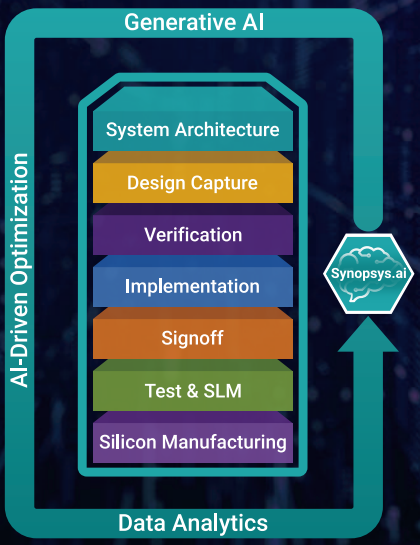

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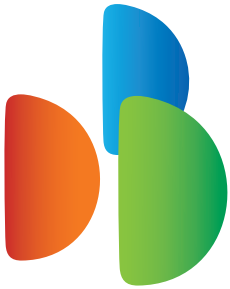

DB GlobalChip

SUNDAY_ OCTOBER 12, 2025

From	Till	LOBBY 2F	Sydney 2F	Grand Ballroom 2F	Napoli 2F	Venice 2F	Miami 2F	Capri 2F	Sicily 1F
12:00	13:00	On-site Registration							
13:00	14:00		Tutorial 1					Tutorial 4	
14:00	15:00		Tutorial 2						
15:00	16:00		Tutorial 3					Tutorial 5	
18:00	20:00	**Welcome Reception** (Sicily Room 1F)							

MONDAY_ OCTOBER 13, 2025

From	Till	LOBBY 2F	Sydney 1+2 2F	Grand Ballroom 2F	Napoli 2F	Venice 2F	Miami 2F	Capri 2F	Sicily 1F
9:30	10:00								
10:00	10:20			**Opening Ceremony** (2F Grand Ballroom)					
10:30	11:20			**Keynote-1 (50mins)** (2F Grand Ballroom)					
11:20	11:30			**Break** (10min.)					
11:30	12:20			**Keynote-2 (50mins)** (2F Grand Ballroom)					
12:20	13:30			**Lunch** (70min.) (2F Grand Ballroom)					Young Professional
13:30	13:45				38	6	14	69	17
13:45	14:00			**Industrial Session 1**	128	112	26	108	42
14:00	14:15	**Sponsor Exhibition**			**DI 1** 223	**AM 1** 234	**AI 1** 134	**SS1** 141	**SS2** 121
14:15	14:30				230	263	153	161	137
14:30	14:45	On-site Registration	Poster Exhitibion (1) **Poster**		248	290	259	169	245
14:45	15:00			**Break & Poster Standing Exhibition Time (15mins)**					
15:00	15:15				9	8	19	64	15
15:15	15:30				49	32	44	68	16
15:30	15:45				**DI 2** 195	**AM 2** 154	**AI 2** 91	**SS3** 76	**SS4** 28
15:45	16:00				239	193	171	110	133
16:00	16:15				282	291	292	155	249
16:15	16:30			**Break & Poster Standing Exhibition Time (15mins)**					
16:30	16:45					33	48	41	24
16:45	17:00	**Live Demo**				46	109	104	30
17:00	17:15					**AM 3** 113	**AI 3** 220	**RF 1** 177	**SS5** 45
17:15	17:30					244	262	252	50
17:30	17:45					246	331	297	127
17:45	18:00	Break Time (15min.)							
18:00	20:00	**Banquet** (2F Grand Ballroom)							

TUESDAY_ OCTOBER 14, 2025

From	Till	LOBBY 2F	Sydney 1+2 2F	Grand Ballroom 2F	Napoli 2F	Venice 2F	Miami 2F	Capri 2F	Sicily 1F
9:00	9:15				149	95	22	60	132
9:15	9:30				164	105	65	74	209
9:30	9:45				199	165	190	81	219
9:45	10:00				**DI 3** 216	**PE** 201	**AI 4** 217	**SS6** 173	**SS7** 229
10:00	10:15				218	251	222	202	242
10:15	10:30				349	266	293	261	277
10:30	10:40			Break (10min.)					
10:40	11:30			**Keynote-3 (50mins)** (2F Grand Ballroom)					
11:30	12:20			**Keynote-4 (50mins)** (2F Grand Ballroom)					
12:20	13:30			Lunch (70min.) (2F Grand Ballroom)					
13:30	13:45			18	83	129	118		21
13:45	14:00			174	125	148	138		54
14:00	14:15	On-site Registration	Poster Exhitibion (2) **Poster**	**AM 4** 183	**RF 2** 241	**AM 5** 159	**BM** 167	**AutoCAS**	**SS8** 299
14:15	14:30			267	273	236	188		304
14:30	14:45			296			276		336
14:45	15:00			**Break & Poster Standing Exhibition Time (15mins)**					
15:00	15:15				55	61	97		39
15:15	15:30				62	67	283		77
15:30	15:45			**Industrial Session 2**	**CM** 85	**AM 6** 140	**SN** 82	**AutoCAS**	**SS9** 124
15:45	16:00				142	156	103		146
16:00	16:15				231	158	237		265
16:15	16:30			**Break & Poster Standing Exhibition Time (15mins)**					
16:30	16:45				98	11	106		90
16:45	17:00			**Industrial Session 3**	135	71	150	**AutoCAS**	**Prime Asia** 301
17:00	17:15				**DI 4** 160	**AM 7** 93	**AI 5** 221		335
17:15	17:30				228	189	253		360
17:30	17:45				281	258	338		363
17:45	18:20	Break Time (25min.)							
18:20	21:00	**Farewell Reception** (Haeundae Byeolbam)							

WEDNESDAY_ OCTOBER 15, 2025								
		LOBBY	Sydney 1+2	Grand Ballroom	Napoli	Venice	Miami	Capri	Sicily
From	Till	2F	2F	2F	2F	2F	2F	2F	1F
10:00	17:00	**Committee Meeting & Industry–University–Research Collaboration Roundtable**							

Regular Sessions			
DI 1	Advanced Digital Circuit Design	AI 1	Lightweight AI/ML Systems
DI 2	Crypto & Fault-Tolerant Systems	AI 2	AI/ML Accelerators
DI 3	Digital Signal Processing Accelerators	AI 3	AI/ML Algorithms
DI 4	Computation Optimization	AI 4	PIM/CIM Systems
AM 1	Analog and Mixed Signal Systems	AI 5	Emerging AI/ML Solutions
AM 2	SAR ADCs and its Building Blocks	RF 1	High Performance RF/mm-Wave Oscillators
AM 3	Delta-Sigma ADCs and Power Conversion Techniques	RF 2	RF Transceivers and Building Blocks
AM 4	Analog Amplifiers and Filters	PE	Power and Energy Circuits and Systems
AM 5	High-speed Wireline Techniques	BM	Biomedical Circuits and Systems
AM 6	Emerging Computing Systems	CM	Beyond CMOS: Nanoelectronics and Hybrid Systems Integration
AM 7	Sensors and Precision References	SN	Sensory, Neural, and Nonlinear Circuits and Systems

Special Sessions	
SS 1	Advanced RF Transceiver Circuits for Next-Generation Wireless Systems
SS 2	Circuits and Applications for Energy-Efficient Edge Systems
SS 3	Display Driver and Touch Readout Circuits
SS 4	Software-Hardware Co-Design for Neural Networks
SS 5	Next-Generation Circuit Techniques: From Analog and Power to Digital Compute
SS 6	Neural Modeling, AI Techniques, and Nonlinear Circuits in Emerging Technologies (6 papers)
SS 7	Wearable Circuits & Systems for Quality-of-Life: Innovations in GeronCAS (6 papers)
SS 8	Energy-Efficient Hardware Architectures for Advanced Edge Computing Applications
SS 9	Recent Advances and Design Trends in Power Management Ics

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